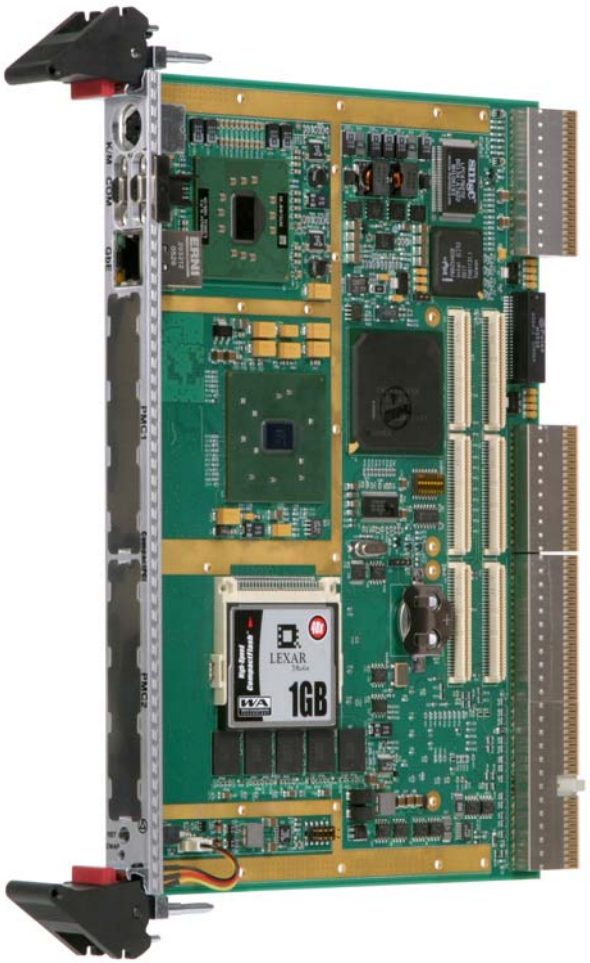
CPM1/CRM1 cPCI Pentium M Based Single Board Computer

User's Manual



CPM1 User's Manual Rev. 1.01

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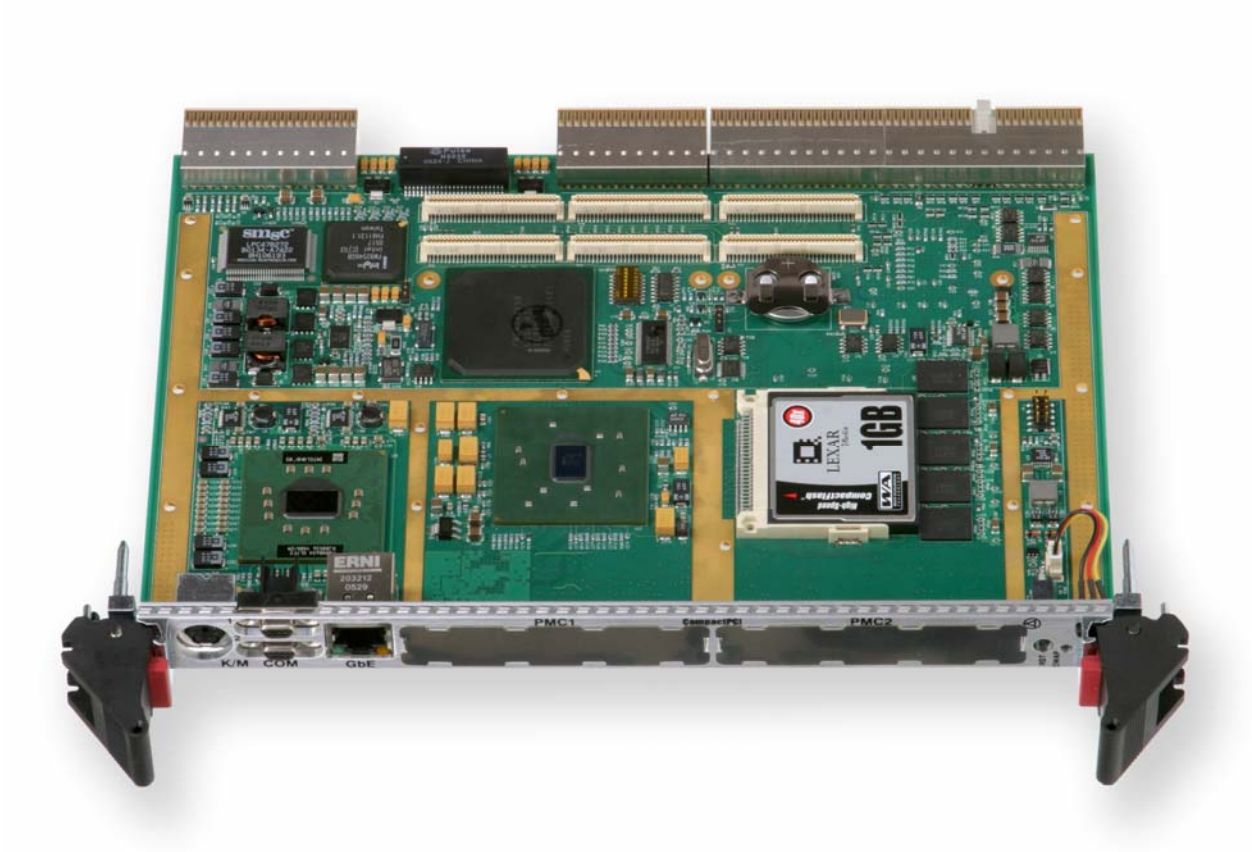
1. Features

The Dynatem CPM1 is a single-slot 6U cPCI Single Board Computer (SBC). The CPM1 offers full PC performance with a Pentium M low-power processor. The CPM1 is available in two versions: the lower cost CPM1 for standard industrial applications and the 1101.2 compliant, conduction-cooled CRPM1 with wedgelocks, stiffener bar, and a full board heatsink for rugged applications. When referring to attributes of both versions, we will use the name CPM1. The CPM1 employs Intel's embedded technology to assure long-term availability.



Features of the CPM1 include:

- Single-slot cPCI operation with on-board CompactFlash disk for bootable mass storage and front panel connectors for two RS232/485 COM ports, a 1 Gb Ethernet port, I/O for two PMC sites, and PS/2 Mouse/Keyboard ports.

- Primary IDE, DVI-I graphics, four USB 2.0 ports, two Serial ATA ports, and Super I/O generated Floppy Disk drive interface and undriven COM3 & 4 ports are routed out to the backplane via the J5 connector

- Two Gb Ethernet ports (in compliance with PICMG 2.16) and PMC I/O for Slot B (in compliance with PICMG 2.3 R1.0) are routed to J3

- The Intel® 855GME Graphics Memory Controller Hub (GMCH) and Intel® 6300ESB I/O Controller Hub (ICH) provide high-speed memory control, built-in graphics, integrated I/O including Serial ATA, USB 2.0, IDE supporting Ultra 100 DMA Mode for transfers up to 88.88 MB/sec, and 64 bit PCI-X bus transfers at 66 MHz
- Intel's 82541 10/100BaseTX interface accessible at the front panel
- Intel's 82546 Ethernet Controller offers two 10/100/1000BaseTX support routed to J3 in compliance with PICMG 2.16 for backplane fabric switching
- Up to 1 GB of DDR DRAM provided on-board
- PLX PCI6254 dual mode Universal asynchronous 64 bit 66 MHz PCI-PCI bridge lets the CPM1 act as a peripheral card or system slot module
- Pigeon Point's IPM Sentry offers IPMI system management in compliance with PICMG 2.9
- Two PCI Mezzanine Card (PMC) expansion sites are supported: one supports up 64 bits @ up to 66 MHz while the other supports 32 bit modules at 33 MHz
- Secondary IDE port for CompactFlash on-board for flash-based mass storage for single-slot booting
- General Software's flash-based system BIOS
- PXE for diskless booting over Ethernet
- Operating System (OS) and driver support, including Windows NT, Embedded NT, XP, QNX, VxWorks, Linux, Solaris, and pSOS+

2. Related Documents

Listed below are documents that describe the Pentium processor and chipset, and the peripheral components used on the CPM1. Either download from the Internet or contact your local distributor for copies of these documents.

The CPM1 uses the Low Voltage Pentium M. For information on this processor, go to:

http://www.intel.com/design/intarch/pentiumm/pentiumm.htm

For the ICH component in the 6300ESBchipset get the *Intel ® 6300ESB I/O Controller Hub Datasheet*. It is document number 300641-003.

http://www.intel.com/design/intarch/datashts/300641.htm

For the GMCH component in the chipset get the *Intel ® 855GM/855GME Chipset Graphics and Memory Controller Hub (GMCH) Datasheet*. It is document number 252615-005:
.
http://www.intel.com/design/chipsets/datashts/252615.htm

For data sheets on I/O controllers:

- *82546EB Fast Ethernet PCI Controller*
  http://developer.intel.com/design/network/products/lan/controllers/82546.htm

- *82541EI Ethernet PCI Controller*
  http://developer.intel.com/design/network/products/lan/controllers/82541ei.htm

- *CompactPCI Specification PICMG 2.0 R3.0 and other CompactPCI Specifications:*
  http://www.picmg.org/compactpci.stm#CompactPCISpecifications

The following documents provide information on the PC architecture and I/O:

- *PCI Local Bus Specification, Revision 2.2*
  http://www.pcisig.com/specifications/

- *PCI-X Specification, Revision 1.0A*
  http://www.pcisig.com/specifications/

- *System Management Bus Specification (SMBus), Revision 1.1*
  http://www.smbus.org/specs/

- *Universal Serial Bus Specification*
  http://www.usb.org/developers

The following documents cover topics relevant to the cPCI and can be purchased through VITA:

- IEEE Std 1014-1987, *IEEE Standard for a Versatile Backplane Bus: cPCI*
  The Institute of Electrical and Electronic Engineers
  345 East 47th Street
  New York, NY 10017
  (800) 678-4333

The following documents are the current draft standards for the PCI Mezzanine Card (PMC):

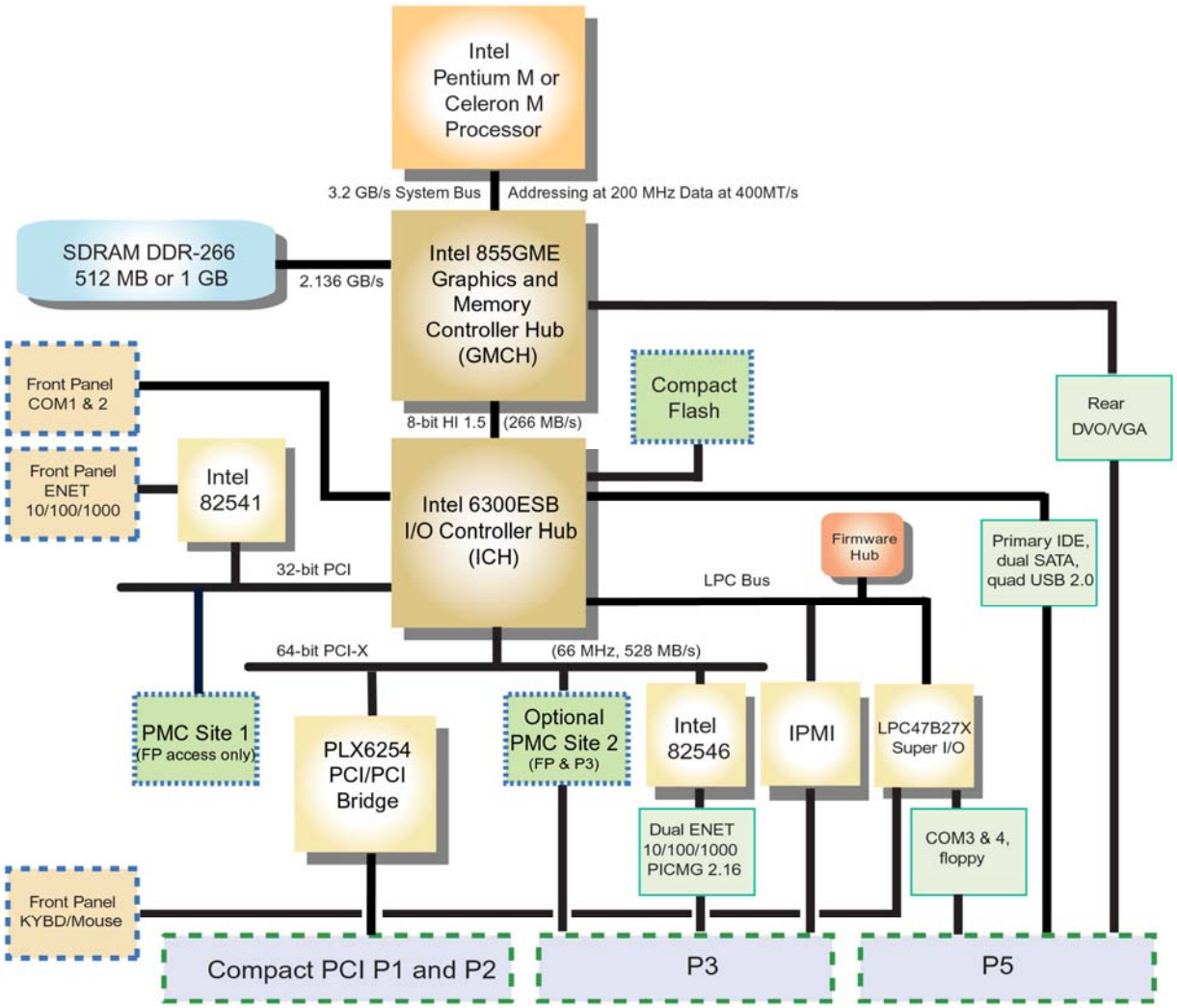
- IEEE Draft Std P1386/2.0, *Draft Standard for a Common Mezzanine Card Family: CMC*
  The Institute of Electrical and Electronic Engineers
  345 East 47th Street
  New York, NY 10017
  (800) 678-4333

- IEEE Draft Std P1386.1/2.0, *Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC*
  The Institute of Electrical and Electronic Engineers
  345 East 47th Street
  New York, NY 10017
  (800) 678-4333

3. Hardware Description

3.1 Overview

The block diagram of the CPM1 is shown below. The sections that follow describe the major functional blocks of the CPM1.



3.2 Processor

The CPM1 supports a Pentium M processor at 1.4 GHz. The Intel Pentium M processor with 2 MB of L2 cache is meet the current and future demands of high-performance, low-power embedded computing, making it ideal for communications, mobile applications, vehicles, and industrial automation applications. While incorporating advanced processor technology, it remains software-compatible with previous members of the Intel® microprocessor family.

- 400 MHz front side bus.
- 4 MB of L2 cache for fast large-table look-ups: routing tables.
- Advanced branch prediction, Micro-op fusion, Hardware stack manager for faster processing.
- Second-generation Streaming SIMD Extensions (Streaming SIMD Extensions 2) capability adds 144 new instructions, including 128-bit SIMD integer arithmetic and 128-bit SIMD double-precision floating-point operation.
- Fully compatible with existing Intel® Architecture-based software.

For further information on the Pentium M processor available from Intel Corporation, search at:

http://www.intel.com/design/intarch/pentiumm/pentiumm.htm

The Intel® Pentium® M processor was designed from the ground up with a new microarchitecture that delivers high performance with low power consumption. With its 90 nm processing technology and 2 MB of L2 advanced transfer cache, the Pentium M offers more performance per Watt.

The Pentium M also offers a dedicated hardware stack manager that employs sophisticated hardware control for improved stack management, advanced branch prediction capability, and a 400 MHz front side bus to the memory controller hub.

3.3 Chipset

The Intel® 855GME Graphics Memory Controller Hub (GMCH) and Intel® 6300ESB I/O Controller Hub (ICH) chipset create an optimized integrated graphics solution with a 400 MHz system bus and integrated 32-bit 3D core at 133 MHz.

The 855GME (GMCH) provides a 266 MHz interface to DDR RAM (72 bits wide with ECC). The CPM1 can be populated with one or two banks of DRAM for 512 MB or 1 GB of total memory respectively. The GMCH system memory architecture is optimized to maintain open pages (up to 16-kB page size) across multiple rows. As a result, up to 16 pages across four rows is supported. To complement this, the GMCH will tend to keep pages open within rows, or will only close a single bank on a page miss.

The 855GME also has an advanced integrated graphical display controller. The CPM1 routes the DVO B port through a PanelLink device and this, along with the VGA port, is brought out through the J5 connector to the system backplane. The XPM1RIO rear plug-in card combines the the DVO and VGA ports in a DVI-I connector. The DVO port:

- Provides high-speed, 12-bit interfaces with 165 MHz dot clocks
- Supports DVO devices (TV-Out Encoders, TMDS & LVDS transmitters, etc.) with pixel resolutions up to 1600 x 1200 @ 85 Hz and up to 1048 x 1536 @ 72 Hz

- Compliant with DVI Specification 1.0
- Front side system bus bandwidth of 3.2 GB/s (400 MHz).

The 6300ESB I/O Controller Hub (ICH) provides most of the CPM1's on-board I/O and it's the CPM1's PCI and PCI-X expansion bridge. The ICH is designed as a low-power, high-performance I/O hub that features:

- 64-bit @ 66 MHz PCI-X expansion that is used on the CPM1 for the on-board PMC-X slot, the two Ethernet ports available in compliance with PICMG 2.16, and for the PLX PCI6254 PCI to PCI bridge to the backplane
- 32-bit @ 33 MHz PCI bus that supports the second PMC site and the front panel's Gb Ethernet port
- Four USB 2.0 compliant ports that are routed to the J5 connector to the backplane and to the optional XPM1RIO rear I/O module where industry standard USB connectors are provided
- Integrated IDE controller supports Ultra 100 DMA Mode Transfers for up to 100 MB/sec read cycles and 88.88 MB/sec write cycles for a CompactFlash drive on-board and a primary IDE port that is routed through J5 to the XPM1RIO
- Two Serial ATA ports providing 150 MB/sec data rates are routed through J5
- Standard PC functionality like a battery-backed RTC and 256-bytes of CMOS RAM, Power Management Logic, Interrupt Controller, Watchdog Timer, AC'97 CODEC, Integrated 16550 compatible UART's, and multimedia timers based on the 82C54

For further information, see the documents referenced in Section 2

3.4 DRAM

The CPM1 supports a 72-bit wide, DDR-266 memory interface with memory bandwidth of 2.1 GB/s with ECC. The module can be populated to support 512 MB or 1 GB of DRAM.

3.5 Intel 82546EB Dual Gigabit Ethernet Controller

The CPM1 supports two 10/100/1000BaseTX channels accessible from the backplane. The Intel 82546EB Dual Port Gigabit Ethernet Controller incorporates two full Gigabit Ethernet MAC and PHY layer functions on a single, compact component. The CPM1 uses the PCI-X interface of the ICH to control the 82546EB. Therefore, the front side data path to the dual Ethernet port controller is 64 bits at 66 MHz.

The Intel 82546EB offers the following features:

- 10, 100, and 1000BaseTX support with auto-negotiation
- Dual 64KB configurable RX and TX packet FIFOs
- 128-bit internal data path architecture for low latency data handling and superior DMA transfer rate performance
- Built-in Phyceiver
- Serial EEPROM for non-volatile Ethernet address storage

Both 10/100/1000BaseTX ports of the 82546 device are brought out to the J3 backplane connector in compliance with the PICMG 2.16 specification. PICMG 2.16 lets the user implement fabric switching on the backplane where 2.16 compliant SBC's can communicate with each other and with an external network through switch modules that are located at either end of the backplane. Optionally these two 1 Gb Ethernet ports are brought to industry standard RJ-45 connectors on Dynatem's rear I/O plug-in module (CPM1PTB).

The Intel 82546 contains several PCI configuration registers. It also contains a number of device registers for controlling the Ethernet operation that can be mapped to the memory space or the I/O space. The PCI signals specific to the CPM1's 82546 are shown below:

Intel 82546 Signal	PCI Bus Connection
Bus	2
IDSEL	AD18 (Device 2)
PREQ	PX_REQ1#
PGNT	PX_GNT1#
PIRQ for Port A	PX_IRQ1
PIRQ for Port B	PX_IRQ2

3.6 Intel 82541 Gb Ethernet Controller For A Front Panel LAN Port

The Intel 82541PI offers the following features:

- 10, 100, and 1000BaseTX support with auto-negotiation.
- Independent 64 KB RX and TX FIFO where the apportionment is tunable to the application.
- Transmit TCP segmentation IP, TCP, and UDP checksum offloading.
- Built-in Phyceiver.
- Serial EEPROM for nonvolatile Ethernet address storage.

The 10BaseT/100/1000BaseTX signals are brought out to J9, an RJ-45 connector with built-in magnetics on the front panel. The connector also features three functioning LEDs: for Linkup, Network Activity, and 1 Gb Link. The LEDs are controlled by the Ethernet circuitry. The pin-out for J9 is given in Appendix A.

The Intel 82541 contains several PCI configuration registers. It also contains a number of device registers for controlling the Ethernet operation that can be mapped to the memory space or the I/O space. The 82541 is controlled by the PCI interface of the ICH. The PCI signals specific to the Intel 82541 are shown below:

Intel 82541 Signal	PCI Bus Connection
Bus	3
IDSEL	AD17 (PCI Device 0)
PREQ	REQ1#
PGNT	GNT1#
PIRQ	INTG#

For further information on the 82541, refer to *82541 Fast Ethernet Multifunction PCI/Cardbus Controller*, available from Intel Corporation. Please go to the link at:
http://www.intel.com/design/network/products/lan/controllers/82541ei.htm

3.7 PLX PCI6254 & PC6540PCI-cPCI Interfaces (Section Under Construction)

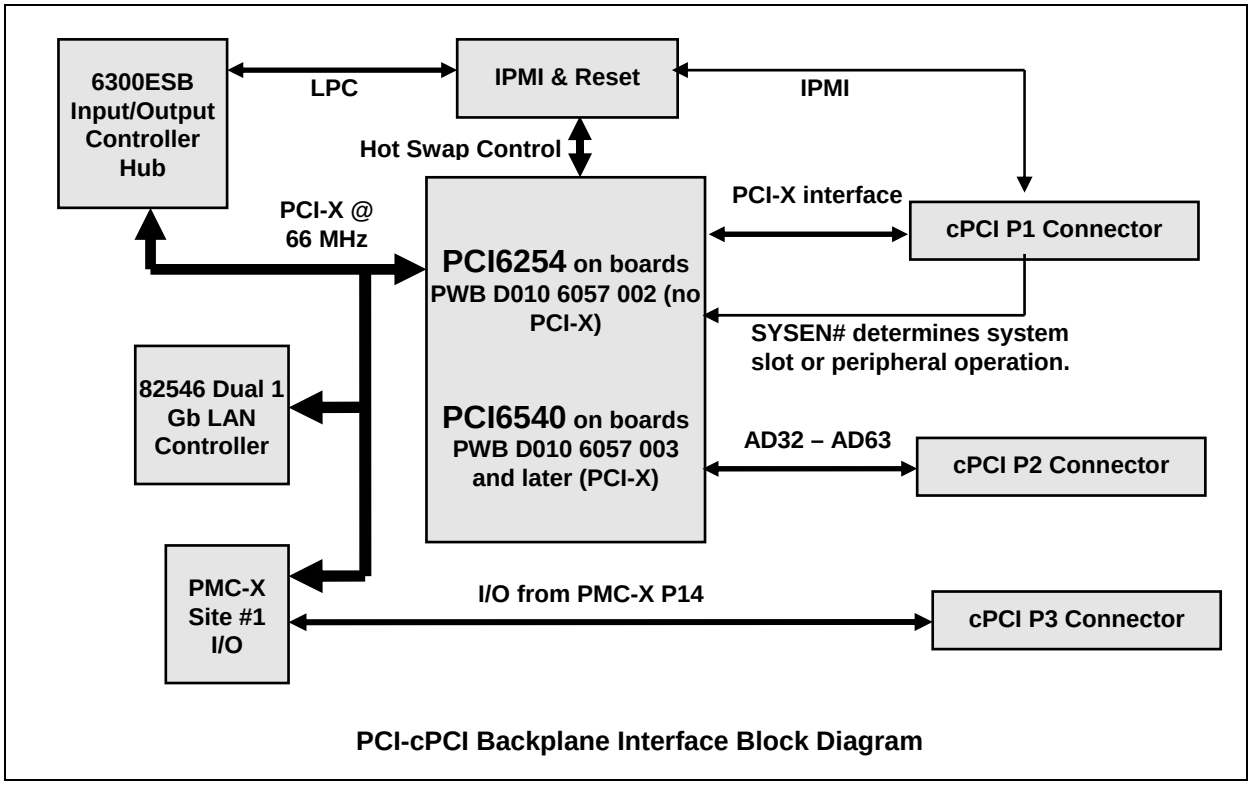
The CPM1 uses two different PCI bridges to the backplane depending on the revision of the module. The first revision of the board (identified by "**PWB 010 6057 002**" etched on the printed circuit board near the top card puller) uses PLX's PCI6254 PCI-PCI bridge.

On subsequent versions of the CPM1 this chip was replaced by the PLX PCI6540 as it supports PCI-X to PCI-X transfers and the primary side of the bridge is shared with the PCI-X compatible 82546 dual 1 Gb Ethernet controller chip and possibly PCI-X compatible PMC modules in PMC site #1. These peripherals cannot operate in PCI-X mode if they share their PCI bus interface with the PCI6254.

The PCI-cPCI interface, based on the PLX PCI 6254 on PWB 010 6057 002, offers the following features:

- 64-bit, 33MHz-66MHz Asynchronous operation
- 1 KB FIFO for efficient PCI-PCI bridging and speed conversion.
- Transparent and non-transparent bridge operation.
- Usable in the cPCI system slot or a peripheral slot.
- Supports hot swapping to eliminate the mid-transaction extraction problems associated with cPCI.

The block diagram of the PCI-PCI interface is shown below:



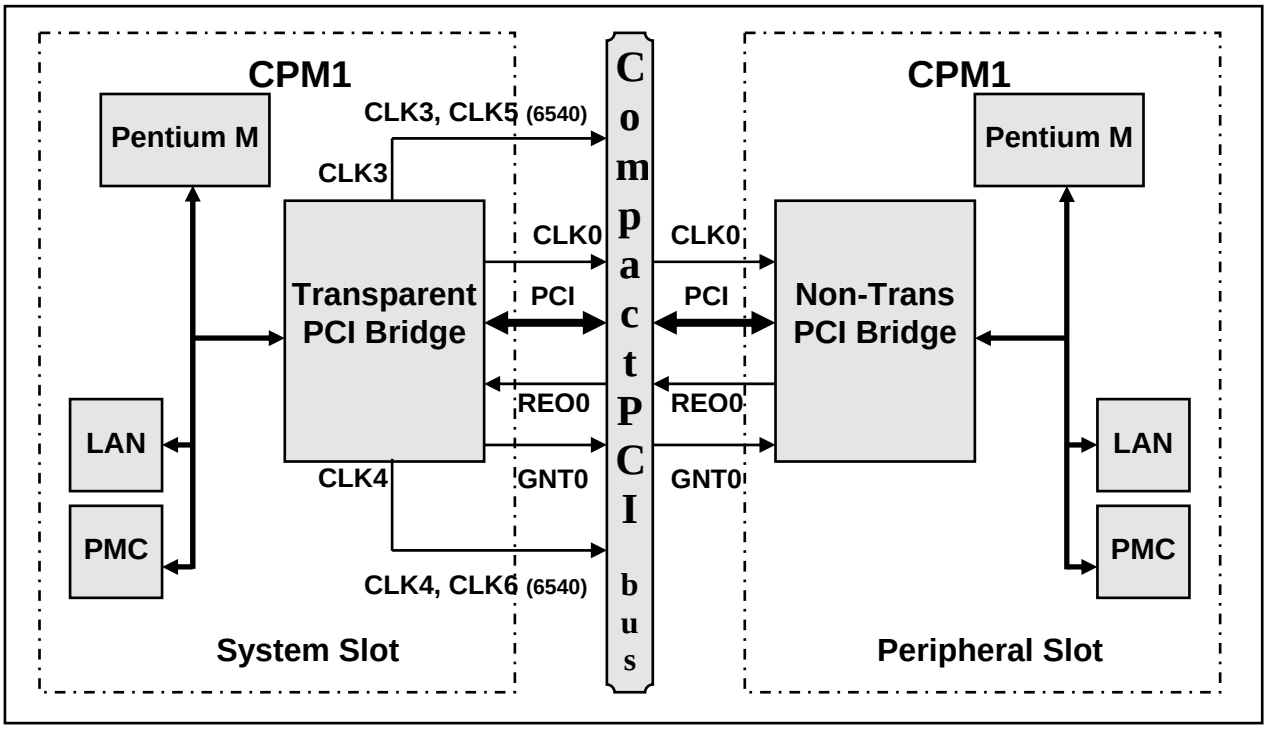
PCI-cPCI Backplane Interface Block Diagram

The PCI-X to cPCI-X interface, based on the PLX PCI 6540, offers the following features:

- 64-bit PCI-X r1.0b compliant asynchronous operation (limited to 66MHz by the 6300ESB south bridge)
- 10 KB FIFO for efficient PCI-X to PCI-X bridging and speed conversion.
- Transparent and non-transparent bridge operation.
- Usable in the cPCI system slot or a peripheral slot.

As shown in the block diagram, the PCI bridge to the backplane shares its primary side with the 82546 Dual Gb Ethernet controller and PMC site #1. If the PMC card installed in site #1 is not PCI-X compatible, then neither the PCI bridge nor the 82546 can operate in the PCI-X mode. The same is true with the bridge chip. Therefore the CPM1 cannot support PCI-X on site #1 PMC cards or on the 82546 on boards that use the PCI6254. The same is true with clock frequencies: the PCI bus can only run as fast as the slowest device on the bus so a PMC module running at 33 MHz will force the 82546 and the PCI-PCI bridge to operate at 33 MHz.

Both the 6254 and the 6540 are universal bridges, meaning their mode of operation is determined by the SYSEN# signal on the cPCI backplane. In this application, the CPM1 can be used without jumpers for the system slot or peripheral slot in a CompactPCI system. The bridge senses the type of slot (system or peripheral) and configures itself as *Transparent* or *Non-Transparent* respectively. In the system slot, the CPU is expected to operate as a host, and the bridge operates in Transparent mode. In the peripheral slot, the CPU is part of an intelligent subsystem, and the bridge is configured in Non-Transparent mode. The figure below shows:



This drawing shows how the CPM1 operates differently depending on whether it's in the system slot on the backplane (denoted by a triangle) or one of the remaining peripheral slots (denoted by circles silkscreened on the backplane). When in the system slot the six additional REQ/GNT pairs and six additional clocks are routed to the backplane in compliance with the PICMG CompactPCI spec (though boards using the PCI6540 route CLK3 to the pins assigned to CLK3 and CLK5 and CLK4 to CLK4 and CLK6 because the 6540 only has five CLK output lines

available). These additional CLK and REQ/GNT lines are not used when the CPM1 is installed in a peripheral slot. They are in a tristate mode.

A *transparent* PCI bridge is meant to provide electrical isolation to the system. It allows additional loads (and devices) to be attached to the bus, and can also be used to operate dissimilar PCI Bus data widths and speeds on the same system. *For example*, a transparent bridge can allow several 32-bit, 33 MHz PCI devices to attach to a 64-bit, 66 MHz PCI-X slot. A *non-transparent* PCI bridge offers address isolation in addition to electrical isolation. Devices on both sides of the bridge retain their own independent Memory space, and data from one side of the bridge is forwarded to the other side, using an address translation mechanism. A non-transparent bridge is used when there is more than one intelligent entity (*such as* multiple processors) in the system. It is a common mechanism used for creating intelligent I/O cards and multi-processor systems.

The bridge is CompactPCI Hot Swap *Ready*, and complies with *PICMG 2.1 R2.0* with *High Availability* Programming Interface level 1 (PI = 1).

The CPM1 reset circuitry is tied to the bridge, since the CPM1 can generate the cPCI SYSRESET* signal as well as be reset by another cPCI board that asserts the SYSRESET* signal. The CPM1 reset circuitry is discussed in detail in Section 3.12.

This section supplements the PCI-to-PCI Bus Bridge documentation (downloadable from PLX Technology's website at http://www.plxtech.com/products/fastlane_bridges/default.asp), which contains comprehensive descriptions of the operation and programming of the PCI 6254 and PCI6540 devices.

3.8 PCI-X Mezzanine Card (PMCX) and PMC Expansion

The CPM1 has two PMC I/O expansion slots: one 64-bit PCI-X compatible site and one 32-bit at 33 MHz site.

The CPM1 supports a PCI-X Mezzanine Card (PMC) site on-board where the I/O can be routed out through the J3 connector (please see Appendix A) or accessed from the front panel. This first PMC site shares its PCI-X bus with the PCI bridge to the backplane and with the 82546GB dual 1 Gb Ethernet controller that provides two PICMG 2.16 compliant LAN ports through J3 to the backplane. This site supports 64-bit PCI-X transfers at 66 MHz. 33 MHz PMC cards or PMC cards not capable of PCI-X transfers can be used in this site but they will limit the 82546GB and the PCI bridge to their capabilities – see Section 3.7.

The CPM1 also provides a 32-bit @ 33 MHz PMC site that shares its PCI bus with the 82541PI front panel Ethernet port. I/O is only accessible from the front panel – it is not routed to the backplane as with the PMC site.

Both sites are compliant with ANSI/VITA 20-2001 for conduction-cooled systems. Conduction cooled PMC modules are recommended for use with the CRPM1 rugged version.

3.9 Intel's FW82802AC Firmware Hub Holds the System BIOS In Flash Memory

The Intel FW82802AC uses a 5-pin interface and provides 1 MByte of flash memory for the system BIOS. This device can fill the 1 MB real mode memory map so only a portion its upper 256 MB is used. The FW82802AC's 1 MB of memory space is segmented into sixteen parameter blocks of 64 KB each. The CPM1 powers up into real mode and the BIOS is eventually shadowed into system DRAM after booting through the BIOS.

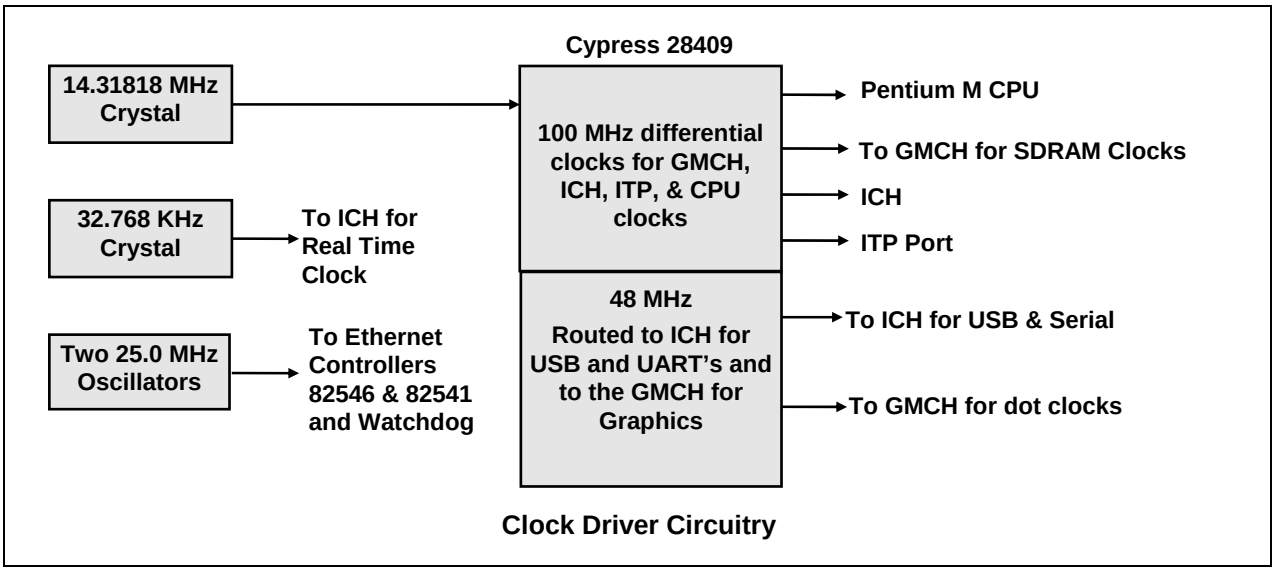
The 6300ESB Southbridge provides the 5-pin interface to the E82802AC. The upper 256 KB of the E82802AC is located from 000C0000 - 000FFFFF and its full 1 MB of memory is aliased from FFF00000 – FFFFFFFF where it can be fully accessed after booting up through the BIOS.

Here's a link to a datasheet for the 82802AC:

ftp://download.intel.com/design/chipsets/datashts/29065804.pdf

3.10 Clock Drivers

The clock driver circuitry is shown below:



Clock Driver Circuitry

The clocks are generated by the Cypress 28409, which is driven by a 14.31818 MHz crystal. DRAM clocks are synthesized by the GMCH and Hub Interface and PCI(-X) clocks are produced by the ICH. A 32.768 KHz Crystal drives the Real Time Clock (RTC) on the ICH. The Fast Ethernet port provided to the front panel by the 82541 and the two 1 Gb Ethernet ports provided to the backplane by the 82546 require separate 25.0 MHz oscillators (one of the two oscillators is also used for the watchdog timer clock). A 64.0 MHz oscillator drives the PCI 6254cPCI circuitry.

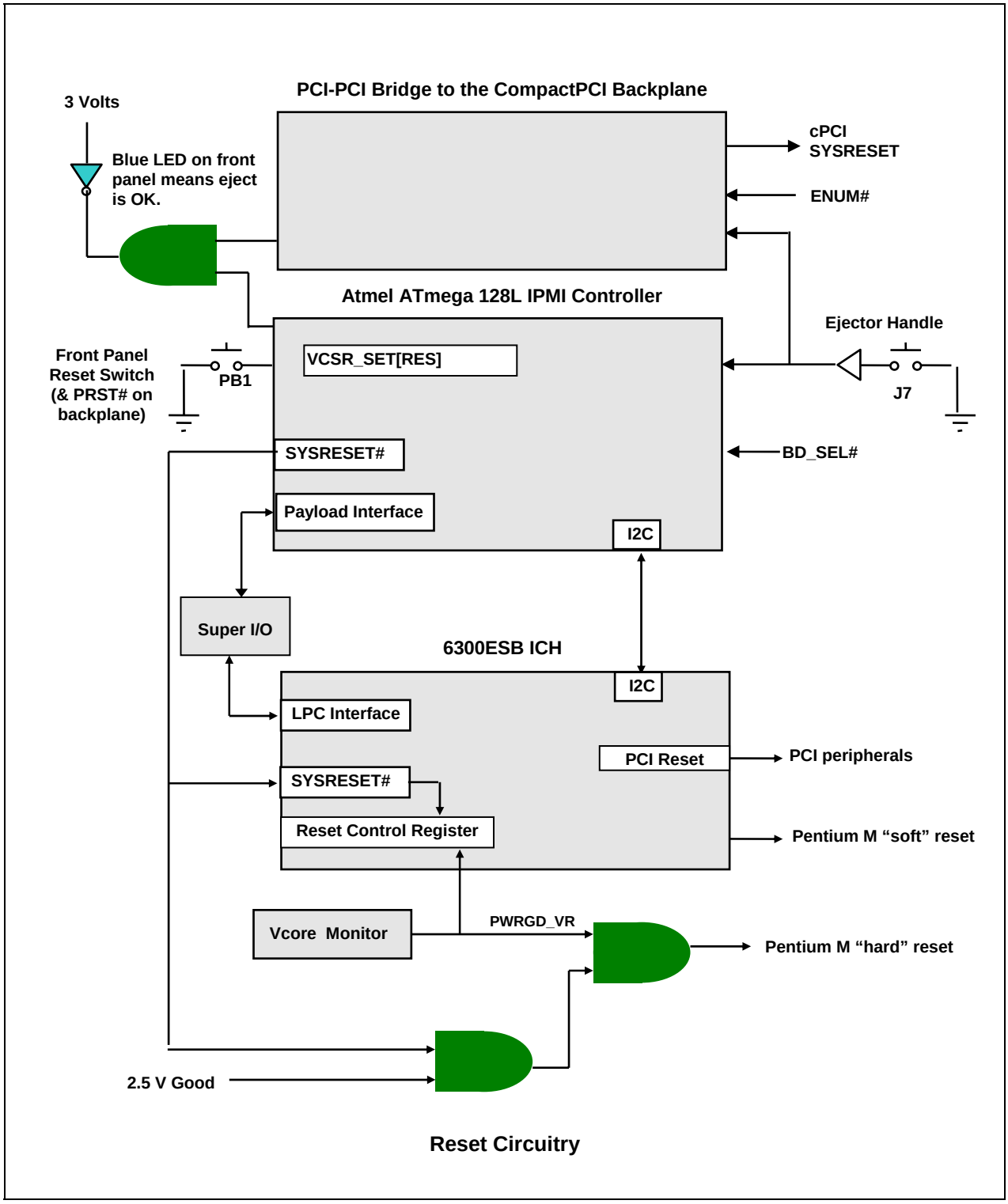
3.11 IPMI & Reset Circuitry & LEDs

The CPM1, with Pigeon Point System's Data Sentry system, implements the mandatory management interfaces defined by the PICMG 2.9 specification to be supported in connection with an IPM Controller.

Optional features are listed below. Several of these signals are required to be supported in cPCI boards that comply with specific PICMG 2.x specifications (such as PICMG 2.1 or PICMG 2.16 for the first four signals below), but with no corresponding requirement that the IPM Controller on a board have any particular responsibility or control regarding them.

- BD_SEL# signal
- Handle switch
- Hot swap LED
- HEALTHY# signal
- Fan control and monitoring

The reset circuitry is shown below:



Reset Circuitry

There are multiple ways to perform a hard reset of the CPM1:

- A simple power cycle (turn the chassis' power off and on).
- There are two options for using a push button reset: the momentary push button switch that's accessible at the CPM1's front panel near the lower ejector handle; the PRST# signal on the backplane (connector J2, pin C17) that is generally connected to the chassis' reset button.
- When the CPM1 is installed in a peripheral slot it can be reset by the system controller module through a conventional PCI Reset.
- A DS1233 monitors the on-board 3.3 VDC, regulated from the 5.0 VDC off the backplane, and provides proper power sequencing for the CPU.
- A hot swap removal of the CPM1 from the chassis. When the ejector handles are released and the blue front panel LED is lit, the board has been reset and it it safe to remove the CPM1 completely from the chassis

For further information on the peripherals that play a part in the reset circuitry, refer to ICH datasheet that's referenced in Section 2.

There are four FRU LEDs that are routed from the IPMI controller and they are located near the front panel on the solder side of the CPM1 under PMC site #2. These LEDs cannot be seen when through the front panel. Here is the signal – LED correspondence:

Atmel ATmega 128L IPMI Controller Pin	LED
MOSI/PB2	D11 Green
MISO/PB3	D11 Red
OC0/PB4	D12 Green
OC1/PB5	D12 Red

4. Installation

The following sections cover the steps necessary to configure the CPM1 and install it into a cPCI system for single-slot operation. This chapter should be read in its entirety before proceeding with the installation.

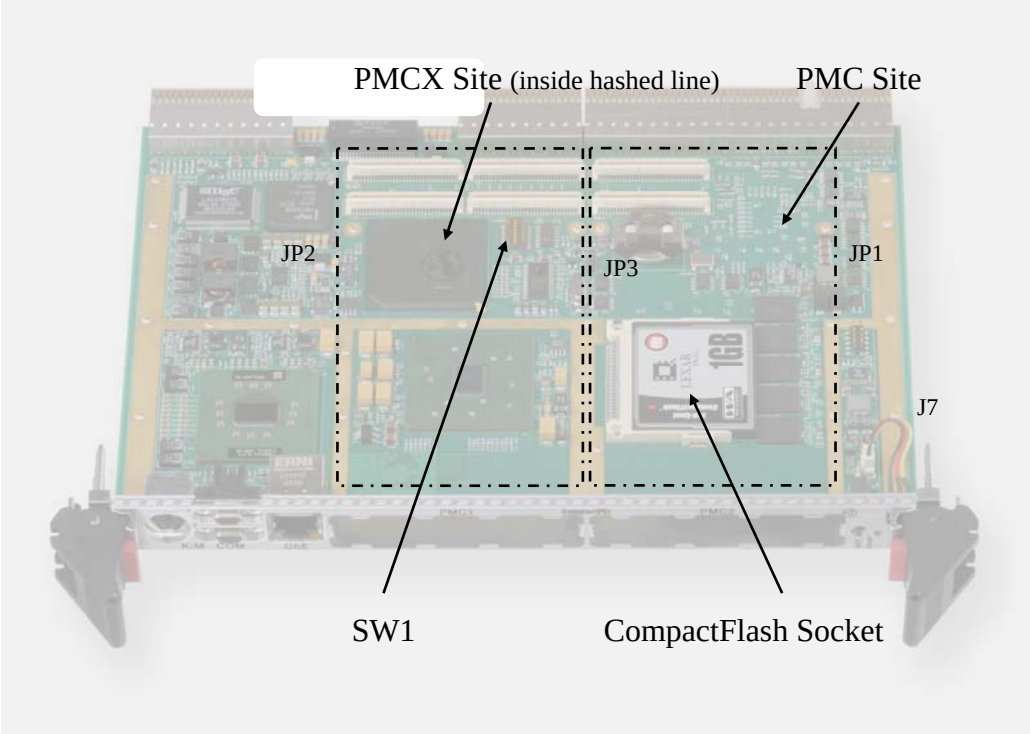
This section explains how to set up user configurable switches and jumpers and how to install CompactFlash drives and PMC modules. The CPM1 is shipped in an antistatic bag. Be sure to observe proper handling procedures during the configuration and installation process, to avoid damage due to electrostatic discharge (ESD).

4.1 Installing the CPM1 in a CompactPCI Chassis

The CPM1 features a Universal PCI(-X)-PCI(-X) bridge to the backplane. Without changing any jumpers the CPM1 will operate as a system slot card (coming up in transparent mode whereby it can initialize peripheral cards on the backplane) when installed in the system slot or as a peripheral card in peripheral slots (coming up in non-transparent mode so that initialization will be done locally without interference from the system slot processor board).

4.2 Jumper Selectable Options

The CPM1 contains three jumpers and a surface-mount piano switch for system configuration. The jumper, switch, PMC site, and CompactFlash socket are indicated in the photo below:



The CPM1 offers a number of user configurable hardware options.

Jumpers	Description
JP1	Grounds PRV_DEV/XB_MEM when shunted
JP2	Determines VIO for the PMCX site #1 (1 – 2 for 3.3 VDC; 2 – 3 for 5.0 VDC)
JP3	Determines VIO for the PMC site #2 (1 – 2 for 3.3 VDC; 2 – 3 for 5.0 VDC)
SW1-1	COM1 is in RS-232 mode when closed; RS-4xx when open
SW1-2	COM2 is in RS-232 mode when closed; RS-4xx when open
SW1-3 through SW1-6	Unused
SW1-7	Close momentarily to flush RTC and NV-RAM and revert to BIOS defaults
SW1-8	**MUST STAY CLOSED** (on-board BIOS is disabled when open)

Jumper JP1 determines the status of PRV_DEV/XB_MEM.

PRV_DEV(when in the Transparent Mode):
When set to 1, the PCI 6540 can mask secondary devices using IDSEL connected to S_AD[23:16] as private devices. Any Type 1 Configuration access to these IDSELs is routed to AD24. If there is no device on S_AD24, the re-routed Type 1 Configuration cycles are Master Aborted. The PCI 6540 also reserves Private Memory space for the secondary port. The Memory space can be programmed using the Private Memory Base and Limit registers (Base—PVTMBAR; PCI:6Ch and VTMBARU32; PCI:70h, Limit—VTMLMT; PCI:6Eh and PVTMLMTU32; PCI:74h). If the limit is smaller than the base, Private Memory space is disabled. The primary port cannot access this Memory space through the bridge and the secondary port does not respond to Memory cycles addressing this Private Memory space.

XB_MEM(when in the Non-Transparent Mode):
When set to 1, the PCI 6540 automatically claims 16 MB of Memory space. This allows the boot-up of the Low-Priority Boot port to proceed without waiting for the Priority Boot port to program the corresponding Memory Base Address registers (BARs). Although the default claims 16 MB, the BARs can be modified by serial EEPROM or software to change the window size. If XB_MEM=1, the P_PORT_READY or S_PORT_READY mechanism is not relevant. Also, if XB_MEM=1, the PCI 6540 autoloads serial EEPROM data up to Group 5 instead of Group 4.
.

PRV_DEV/XB_MEM	JP1
Grounded, Logic 0	Closed
Logic 1	Open

PMCX Site #1 Signaling Voltage Selection

Jumpers JP2 & JP3 select the VIO routed to the CPM1's PMCX & PMC modules respectively. The VIO pins determine the signaling voltage on the PMC(X) modules' PCI(-X) interface. Refer to the PMC module's reference manual to ascertain the recommended VIO. Shunting pins 1 & 2 of JP2 & JP3 provides a VIO of 3.3 VDC. Shunting between pins 2 & 3 routes 5 VDC to the VIO pins on the PMC(X) module.

VIO Voltage Level	JP2
3.3 VDC (Necessary for PCI-X Operation)	1-2
5 VDC	2-3

PMCX Site #1 Signaling Voltage Selection

VIO Voltage Level	JP3
3.3 VDC	1-2
5 VDC	2-3

PMC Site #2 Signaling Voltage Selection

The SW1 switches are closed when in the "on" position.

Switch SW1-1 determines the communication mode under which the CPM1's COM1 port will operate, RS-232 or RS-422/485.

COM1 Mode Selection	SW1-1
RS-4xx Mode	Open
RS-232 Mode	Closed

COM1 Selection

Switch SW1-2 determines the communication mode under which the CPM1's COM2 port will operate, RS-232 or RS-422/485

COM2 Mode Selection	SW1-2
RS-4xx Mode	Open
RS-232 Mode	Closed

COM2 Selection

Switch SW-7 should be closed momentarily (for about 30 seconds) to restore the default BIOS settings. SW1-8 should always be closed (in the "on" position) – this switch is used for factory use.

4.3 CompactFlash Drive Installation

The CPM1 supports a bootable CompactFlash Drive for single-slot booting. Connector J4 is a Type II CompactFlash connector and is used for this purpose. J4 is located behind the front panel Ethernet connector on the CPM1's printed circuit board.

4.4 PCI Mezzanine Card (PMC) Installation

The CPM1 supports two add-on module sites that let the user expand the CPM1's local I/O with PCI Mezzanine Card (PMC) or PMCX (PMC modules capable of PCI-X transfers) cards. Only one of the two sites (located in the middle of the CPM1 and labeled "PMC1" on the front panel) supports PMCX cards that, in turn, support PCI-X transfers at a maximum of 66 MHz. The PMCX site is backwards compatible and can support any module from 32-bit PMC cards at 33 MHz to 64-bit PMCX modules at 66 MHz, however, it shares a bus with the 82546EB dual Gb LAN controller used for PICMG 2.16 compliance and the PCI6540 PCI-X to PCI-X bridge to the cPCI backplane. Putting a standard PMC card in this site will force the 82546EB and the PCI6540 to operate in standard PCI mode.

The CPM1's PCI-X bus interfaces to the 82546 dual Gb Ethernet controller and to the PMCX site.

PMCX site	Available Data Rates with VIO = 5 V (JP3 is shunted between pins 2 & 3)	Available Data Rates with VIO = 3.3 V (JP3 is shunted between pins 1 & 2)
1	33 MHz	33 MHz and 66 MHz

The General Software BIOS will determine during startup what the status is on the installed PMC(X) card. The BIOS monitors the following pins that are routed to the ICH: PCIXCAP (PCX-X capable and it is pin 39 on

connector P11) and M66EN (66 MHz capable and pin 47 on connector P12). The user's manual on your PMC(X) modules will tell you how PCIXCAP (JN1, pin 39) and M66EN (JN2, pin 47) are configured. If either is grounded than the PMC(X) module does not have the corresponding capability (these pins were assigned as ground on the original PMC specification before PCI-X or 66 MHz modes of operation were supported).

Conventionally PMC connectors have four designators: JN1 – JN4. JN1 & JN2 provide all the signals necessary for 32-bit PCI transactions, JN3 has the 32 additional data lines required for 64-bit transfers, and JN4 routes I/O off the module for possible backplane access (see Section A for JN4 to P2 backplane PMCX I/O routing). The following table lists the reference designators used on the CPM1's PMC(X) site:

PMC1 site	JN1	JN2	JN3	JN4
1	P11	P12	P13	P14

The second PMC site, labeled PMC2 on the front panel, only supports 32-bit PCI transactions at 33 MHz. There is no JN3 connector for 64-bit transfers and there's no JN4 connector to route I/O to the backplane. The following table lists the reference designators used on the CPM1's second PMC site:

PMC2 site	JN1	JN2	JN3	JN4
1	P21	P22	N/A	N/A

4.5 Front Panel Connectors and Reset Switch

The CPM1 offers front panel connections for two COM ports, one PS/2 connector for a combined mouse/keyboard interface, and an RJ45 connector for a 1 Gb Ethernet port. The CPM1 is shipped with a splitter cable for the PS/2 mouse and keyboard ports. Install all front panel cables by inserting them into the appropriate connector. Thw COM1 and COM2 ports use Micro D-subminiature connectors that can be secured to the CPM1 by tightening their thumbscrews into the connectors' jackscrews. Ethernet mating connectors should snap into place. Mounting hardware for the front panel connectors are isolated from the CPM1's digital ground. They are continuous with the front panel itself that, in turn, is common with chassis ground.

The CPM1 contains a recessed reset switch, accessible from the front panel. To reset the CPM1, press the reset switch using a small screwdriver blade or similar implement.

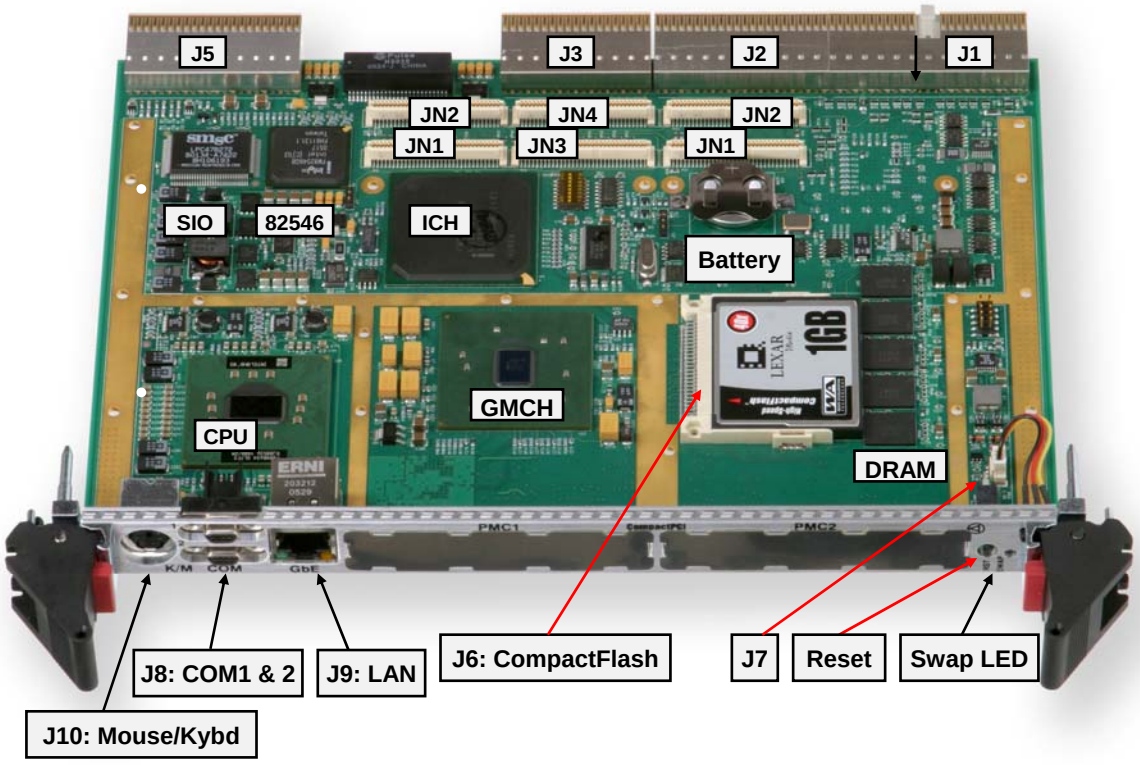
There is also a PICMG 2.1, R2.0 compliant hot swap LED that can be seen at the front panel. This LED goes on when it is safe to extract the CPM1 from its chassis.

The Ethernet connector has a pair of indicator LED's built in. These two LED's offer stats on the 10/100BaseTX port provided by the 82541PI Ethernet controller on the CPM1. Here is an explanation of their functionality:

- **Link** – Ethernet link is established when this LED flashes yellow.
- **1 Gb mode** – Ethernet data is being transmitted at 1 Gbps when this LED flashes green.

A. Connector Pin-outs

The locations of the CPM1 connectors are shown below. The connectors that do not go to the front panel have their pin 1 location designated accordingly.



A.1 COM1 & COM2 Front Panel Connectors (J8)

Connector J8 provides two RS-232 interfaces at the front panel via a stacked pair of Micro D sub-miniature (MDSM) DB-9 connectors. Both connectors have the same pin-out. The connector for COM2 is lower and closer to the printed circuit board.

Pin	RS-232 Signals
1	Data Carrier Detect (DCD) Input
2	Received Data (RxD) Input
3	Transmitted Data (TxD) Output
4	Data Terminal Ready (DTR) Output
5	GND
6	Data Set Ready (DSR) Input
7	Request To Send (RTS) Output
8	Clear To Send (CTS) Input
9	Ring Indicator (RI) Input

COM1 & COM2 Connector (J8) – Front Panel DB9M Connector. The metal shell of the connectors go to chassis ground.

A.2 I Gb Ethernet Front Panel Connector (J9)

The CPM1 uses an RJ45 connector to provide an Ethernet port at the front panel. J9 has a built-in yellow LED for Link and a green LED to indicate 1 Gb mode.

Pin	Signal Description	Signal Description
1	Port A Transmit Data + (TX+)	TP0+
2	A Transmit Data - (TX-)	TP0-
3	A Receive Data + (RX+)	TP1+
4	Unused	TP2+
5	Unused	TP2-
6	A Receive Data - (RX-)	TP1-
7	Unused	TP3+
8	Unused	TP3-

1 Gb Ethernet Connector (J9) – Front Panel RJ-45 Connector. The metal shell of the connector goes to chassis ground.

A.3 CompactFlash Interface Connector (J6)

Pin	Signal	Pin	Signal
1	GND	26	CMPFLASHDET
2	D3	27	D11
3	D4	28	D12
4	D5	29	D13
5	D6	30	D14
6	D7	31	D15
7	CS1#	32	CS3#
8	GND	33	No connection
9	GND	34	DIOR#
10	GND	35	DIOW#
11	GND	36	+5 VDC
12	GND	37	DIRQ (IRQ15)
13	+5 VDC	38	+5 VDC
14	GND	39	Pulled Low (master)
15	GND	40	No connection
16	GND	41	IDERESET
17	GND	42	Pulled Up (DIORDY)
18	DA2	43	No connection
19	DA1	44	+5 VDC
20	DA0	45	No connection
21	D0	46	Pull-up to +5 VDC
22	D1	47	D8
23	D2	48	D9
24	No connection	49	D10
25	No connection	50	GND

CompactFlash Type II Interface Connector (J6)

A.4 PS/2 Mouse/Keyboard Connector (J10)

Pin	Signal Description
1	Keyboard Data
2	Mouse Data
3	GND
4	+5 VDC (via 1 amp self-resetting fuse F1)
5	Keyboard Clock
6	Mouse Clock

Keyboard/Mouse Connector (J10) – Front Panel Mini-DIN Receptacle. The metal shell of the connector goes to chassis ground.

A.5 JTAG Debug Port (J13)

This JTAG connector permits in-circuit emulation for system debugging and is not populated on production boards.

Pin	Signal	Pin	Signal
1	GND	2	GND
3	CPU_BPM0#	4	Pulled Up
5	CPU_BPM1#	6	ITP_RST#
7	CPU_BPM2#	8	GND
9	CPU_BPM3#	10	ITP_TDI
11	CPU_BPM4#/PRDY#	12	ITP_TMS
13	CPU_BPM5#/PREQ#	14	ITP_TRST#
15	FSB_CPURST#	16	ITP_TCK
17	NC	18	Pulled Down
19	ITP_BCLK0	20	GND
21	ITP_BCLK1	22	Pulled Up
23	CPU_BPM5#/PREQ#	24	ITP_TDO
25	GND	26	NC

JTAG Connector (J13)

A.6 cPCI Connectors (J1, J2, J3, and J5)

Connectors J1 and J2 bring a 64-bit 66 MHz capable PCI-X bus to the CompactPCI backplane. "PU" stands for "pulled up".

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A25	5 VDC	B25	REQ64#	C25	ENUM#	D25	3.3 VDC	E25	5 VDC
A24	AD1	B24	5 VDC	C24	VI/OL	D24	AD0	E24	ACK64#
A23	3.3 VDC	B23	AD4	C23	AD3	D23	5 VDC L	E23	AD2
A22	AD7	B22	GND	C22	3.3 VDC L	D22	AD6	E22	AD5
A21	3.3 VDC	B21	AD9	C21	AD8	D21	M66EN	E21	C/BE0#
A20	AD12	B20	GND	C20	VI/O	D20	AD11	E20	AD10
A19	3.3 VDC	B19	AD15	C19	AD14	D19	GND	E19	AD13
A18	SERR#	B18	GND	C18	3.3 VDC	D18	PAR	E18	C/BE1#
A17	3.3 VDC	B17	IPMB SCL	C17	IPMB SDA	D17	GND	E17	PERR#
A16	DEVSEL#	B16	PCIXCAP	C16	VI/O	D16	STOP#	E16	LOCK#
A15	3.3 VDC	B15	FRAME#	C15	IRDY#	D15	BDSEL#	E15	TRDY#
A14	KEY1: NC	B14	KEY4: NC	C14	KEY7: NC	D14	KEY10: NC	E14	KEY13: NC
A13	KEY2: NC	B13	KEY5: NC	C13	KEY8: NC	D13	KEY11: NC	E13	KEY14: NC
A12	KEY3: NC	B12	KEY6: NC	C12	KEY9: NC	D12	KEY12: NC	E12	KEY15: NC
A11	AD18	B11	AD17	C11	AD16	D11	GND	E11	C/BE2#
A10	AD21	B10	GND	C10	3.3 VDC	D10	AD20	E10	AD19
A09	C/BE3#	B09	GND/IDSEL	C09	AD23	D09	GND	E09	AD22
A08	AD26	B08	GND	C08	VI/O	D08	AD25	E08	AD24
A07	AD30	B07	AD29	C07	AD28	D07	GND	E07	AD27
A06	REQ0#	B06	GND	C06	3.3 VDC L	D06	CLK0	E06	AD31
A05	RESVD: NC	B05	RESVD: NC	C05	RST#	D05	GND	E05	GNT0#
A04	IPMB PWR: NC	B04	HEALTHY#	C04	VI/OL	D04	INTP	E04	INTS
A03	INTA#	B03	INTB#	C03	INTC#	D03	5 VDC L	E03	INTD#
A02	TCK: NC	B02	5 VDC	C02	TMS: NC	D02	TDO: NC	E02	TDI: NC
A01	5 VDC	B01	-12 VDC: NC	C01	TRST#: NC	D01	+12 VDC	E01	5 VDC

CompactPCI Backplane Connector (J1) – Row F is grounded

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A22	GA4	B22	GA3	C22	GA2	D22	GA1	E22	GA0
A21	CLK6	B21	GND	C21	RESVD: NC	D21	RESVD: NC	E21	RESVD: NC
A20	CLK5	B20	GND	C20	RESVD: NC	D20	GND	E20	RESVD: NC
A19	GND	B19	GND	C19	RESVD: NC	D19	RESVD: NC	E19	RESVD: NC
A18	RESVD: NC	B18	RESVD: NC	C18	RESVD: NC	D18	GND	E18	RESVD: NC
A17	RESVD: NC	B17	GND	C17	PRST#	D17	REQ6#	E17	GNT6#
A16	RESVD: NC	B16	RESVD: NC	C16	DEG# (Pulled Up)	D16	GND	E16	RESVD: NC
A15	RESVD: NC	B15	GND	C15	FAL# (Pulled Up)	D15	REQ5#	E15	GNT5#
A14	AD35	B14	AD34	C14	AD33	D14	GND	E14	AD32
A13	AD38	B13	GND	C13	VI/O	D13	AD37	E13	AD36
A12	AD42	B12	AD41	C12	AD40	D12	GND	E12	AD39
A11	AD45	B11	GND	C11	VI/O	D11	AD44	E11	AD43
A10	AD49	B10	AD48	C10	AD47	D10	GND	E10	AD46
A09	AD52	B09	GND	C09	VI/O	D09	AD51	E09	AD50
A08	AD56	B08	AD55	C08	AD54	D08	GND	E08	AD53
A07	AD59	B07	GND	C07	VI/O	D07	AD58	E07	AD57
A06	AD63	B06	AD62	C06	AD61	D06	GND	E06	AD60
A05	C/BE5#	B05	64EN#	C05	VI/O	D05	C/BE4#	E05	PAR64
A04	VI/O	B04	RESVD: NC	C04	C/BE7#	D04	GND	E04	C/BE6#
A03	CLK4	B03	GND	C03	GNT3#	D03	REQ4#	E03	GNT4#
A02	CLK2	B02	CLK3	C02	SYSEN#	D02	GNT2#	E02	REQ3#
A01	CLK1	B01	GND	C01	REQ1#	D01	GNT1#	E01	REQ2#

CompactPCI Backplane Connector (J2) – Row F is grounded

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A19	RESVD: NC	B19	RESVD: NC	C19	RESVD: NC	D19	RESVD: NC	E19	RESVD: NC
A18	LPa_DC-	B18	LPa_DC+	C18	GND	D18	LPa_DA-	E18	LPa_DA+
A17	LPa_DD-	B17	LPa_DD+	C17	GND	D17	LPa_DB-	E17	LPa_DB+
A16	LPb_DC-	B16	LPb_DC+	C16	GND	D16	LPb_DA-	E16	LPb_DA+
A15	LPb_DD-	B15	LPb_DD+	C15	GND	D15	LPb_DB-	E15	LPb_DB+
A14	3.3 VDC	B14	3.3 VDC	C14	3.3 VDC	D14	5 VDC	E14	5 VDC
A13	PMCI/O pin 5	B13	PMCI/O pin 4	C13	PMCI/O pin 3	D13	PMCI/O pin 2	E13	PMCI/O pin 1
A12	PMCI/O pin 10	B12	PMCI/O pin 9	C12	PMCI/O pin 8	D12	PMCI/O pin 7	E12	PMCI/O pin 6
A11	PMCI/O pin 15	B11	PMCI/O pin 14	C11	PMCI/O pin 13	D11	PMCI/O pin 12	E11	PMCI/O pin 11
A10	PMCI/O pin 20	B10	PMCI/O pin 19	C10	PMCI/O pin 18	D10	PMCI/O pin 17	E10	PMCI/O pin 16
A09	PMCI/O pin 25	B09	PMCI/O pin 24	C09	PMCI/O pin 23	D09	PMCI/O pin 22	E09	PMCI/O pin 21
A08	PMCI/O pin 30	B08	PMCI/O pin 29	C08	PMCI/O pin 28	D08	PMCI/O pin 27	E08	PMCI/O pin 26
A07	PMCI/O pin 35	B07	PMCI/O pin 34	C07	PMCI/O pin 33	D07	PMCI/O pin 32	E07	PMCI/O pin 31
A06	PMCI/O pin 40	B06	PMCI/O pin 39	C06	PMCI/O pin 38	D06	PMCI/O pin 37	E06	PMCI/O pin 36
A05	PMCI/O pin 45	B05	PMCI/O pin 44	C05	PMCI/O pin 43	D05	PMCI/O pin 42	E05	PMCI/O pin 41
A04	PMCI/O pin 50	B04	PMCI/O pin 49	C04	PMCI/O pin 48	D04	PMCI/O pin 47	E04	PMCI/O pin 46
A03	PMCI/O pin 55	B03	PMCI/O pin 54	C03	PMCI/O pin 53	D03	PMCI/O pin 52	E03	PMCI/O pin 51
A02	PMCI/O pin 60	B02	PMCI/O pin 59	C02	PMCI/O pin 58	D02	PMCI/O pin 57	E02	PMCI/O pin 56
A01	VIO_PX	B01	PMCI/O pin 64	C01	PMCI/O pin 63	D01	PMCI/O pin 62	E01	PMCI/O pin 61

CompactPCI Backplane Connector (J3) – Row F is grounded

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A22	PDD8	B22	PDD7	C22	IRQ14	D22	12 VDC	E22	DVI_CLK+
A21	PDD9	B21	PDD6	C21	PRI_RST#	D21	GND	E21	DVI_CLK-
A20	PDD10	B20	PDD5	C20	SPKR	D20	LINKA#	E20	DVI_HSYNC
A19	PDD11	B19	PDD4	C19	PDDREQ	D19	ACT_A#	E19	DVI_GREEN
A18	PDD12	B18	PDD3	C18	PDIOW#	D18	LINKB#	E18	DVI_RED
A17	PDD13	B17	PDD2	C17	PDIOR#	D17	ACT_B#	E17	DVI_BLUE
A16	PDD14	B16	PDD1	C16	PIORDY	D16	USB_OC0#	E16	DVI_VSYNC
A15	PDD15	B15	PDD0	C15	PDDACK#	D15	USB_OC2#	E15	DVI_DDCDAT
A14	PRI_DET	B14	PDA1	C14	DRVEN0	D14	DVI_DDCLK	E14	DVI_D2+
A13	PDA2	B13	PDA0	C13	DRVEN1	D13	DVI_HPDET	E13	DVI_D2-
A12	PDCS1#	B12	PDCS3#	C12	MTR0#	D12	GND	E12	DVI_D1+
A11	COM4 DCD#	B11	COM3 DCD#	C11	DSKCHG#	D11	FAN_S1	E11	DVI_D1-
A10	COM4 DSR	B10	COM3 DSR	C10	DS0#	D10	FAN_T1	E10	DVI_D0+
A09	COM4 RxD	B09	COM3 RxD	C09	DIR#	D09	FAN_S2	E09	DVI_D0-
A08	COM4 RTS	B08	COM3 RTS	C08	STEP#	D08	FAN_T2	E08	USB_P0N
A07	COM4 TxD	B07	COM3 TxD	C07	WDATA#	D07	FAN_S3	E07	USB_P0P
A06	COM4 CTS#	B06	COM3 CTS#	C06	WGATE#	D06	FAN_T3	E06	USB_P1N
A05	COM4 DTR#	B05	COM3 DTR#	C05	HDSEL#	D05	FAN_S4	E05	USB_P1P
A04	COM4 RI#	B04	COM3 RI#	C04	INDEX#	D04	FAN_T4	E04	USB_P2N
A03	WRTPRT#	B03	RDATA#	C03	TRK0#	D03	SATA_LED#	E03	USB_P2P
A02	SATA1_RXP	B02	SATA1_RXN	C02	SATA1_TXN	D02	SATA1_TXP	E02	USB_P3N
A01	SATA0_RXP	B01	SATA0_RXN	C01	SATA0_TXN	D01	SATA0_TXP	E01	USB_P3P

CompactPCI Backplane Connector (J5) – Row F is grounded

A.7 PCI-X Mezzanine Card (PMCX) Connectors (JN1, JN2, JN3, and JN4)

This section has the pin-outs for all four PMC connectors. On the CPM1 connectors JN1, JN2, JN3, and JN4 are labeled P11, P12, P13, and P14 respectively. This site is labeled PMC1 on the front panel.

Pin	Signal	Pin	Signal
1	5.6K pull-down	2	-12 VDC
3	GND	4	PX_PIRQ0#
5	PX_PIRQ1#	6	PX_PIRQ2#
7	No connection	8	+5 VDC
9	PX_PIRQ3#	10	No connection
11	GND	12	No connection
13	PCI CLK	14	GND
15	GND	16	GNT0#
17	REQ0#	18	+5 VDC
19	VI/O	20	AD31
21	AD28	22	AD27
23	AD25	24	GND
25	GND	26	C/BE3#
27	AD22	28	AD21
29	AD19	30	+5 VDC
31	VI/O	32	AD17
33	FRAME#	34	GND
35	GND	36	IRDY#
37	DEVSEL#	38	+5 VDC
39	PCIXCAP	40	LOCK#
41	No connection	42	No connection
43	PAR	44	GND
45	VI/O	46	AD15
47	AD12	48	AD11
49	AD9	50	+5 VDC
51	GND	52	C/BE0#
53	AD6	54	AD5
55	AD4	56	GND
57	VI/O	58	AD3
59	AD2	60	AD1
61	AD0	62	+5 VDC
63	GND	64	REQ64#

PCI-X Mezzanine Card (PMC1) Connector (P11) – Molex 71439-0164

VIO is jumper selectable (through JP1, please see Section 4.1).

Pin	Signal	Pin	Signal
1	+12 VDC	2	TRST (pulled down)
3	TMS (pulled up)	4	No connection
5	TDI (pulled up)	6	GND
7	GND	8	No connection
9	No connection	10	No connection
11	+3.3 VDC	12	+3.3 VDC
13	PCI RST#	14	GND
15	+3.3 VDC	16	GND
17	No connection	18	GND
19	AD30	20	AD29
21	GND	22	AD26
23	AD24	24	+3.3 VDC
25	AD17 (IDSEL)	26	AD23
27	+3.3 VDC	28	AD20
29	AD18	30	GND
31	AD16	32	C/BE2#
33	GND	34	No connection
35	TRDY#	36	+3.3 VDC
37	GND	38	STOP#
39	PERR#	40	GND
41	+3.3 VDC	42	SERR#
43	C/BE1#	44	GND
45	AD14	46	AD13
47	M66EN	48	AD10
49	AD8	50	+3.3 VDC
51	AD7	52	No connection
53	+3.3 VDC	54	No connection
55	No connection	56	GND
57	No connection	58	No connection
59	GND	60	No connection
61	ACK64#	62	+3.3 VDC
63	GND	64	No connection

PCI-X Mezzanine Card (PMC1) Connector (P12) – Molex 71439-0164

Pin	Signal	Pin	Signal
1	No connection	2	GND
3	GND	4	C/BE7#
5	C/BE6#	6	C/BE5#
7	C/BE4#	8	GND
9	VIO	10	PAR64
11	AD63	12	AD62
13	AD61	14	GND
15	GND	16	AD60
17	AD59	18	AD58
19	AD57	20	GND
21	VIO	22	AD56
23	AD55	24	AD54
25	AD53	26	GND
27	GND	28	AD52
29	AD51	30	AD50
31	AD49	32	GND
33	GND	34	AD48
35	AD47	36	AD46
37	AD45	38	GND
39	VIO	40	AD44
41	AD43	42	AD42
43	AD41	44	GND
45	GND	46	AD40
47	AD39	48	AD38
49	AD37	50	GND
51	GND	52	AD36
53	AD35	54	AD34
55	AD33	56	GND
57	VIO	58	AD32
59	No connection	60	No connection
61	No connection	62	GND
63	GND	64	No connection

PCI-X Mezzanine Card (PMC1) Connector (P13) – Molex 71439-0164

Pin	Signal	Pin	Signal
1	E13	2	D13
3	C13	4	B13
5	A13	6	E12
7	D12	8	C12
9	B12	10	A12
11	E11	12	D11
13	C11	14	B11
15	A11	16	E10
17	D10	18	C10
19	B10	20	A10
21	E9	22	D9
23	C9	24	B9
25	A9	26	E8
27	D8	28	C8
29	B8	30	A8
31	E7	32	D7
33	C7	34	B7
35	A7	36	E6
37	D6	38	C6
39	C6	40	A6
41	E5	42	D5
43	C5	44	B5
45	A5	46	E4
47	D4	48	C4
49	B4	50	A4
51	E3	52	D3
53	C3	54	B3
55	A3	56	E2
57	D2	58	C2
59	B2	60	A2
61	E1	62	D1
63	C1	64	B1

PCI-X Mezzanine Card (PMC1) Site #1 Connector (P14) – Molex 71439-0164

These I/O lines are optionally routed to the cPCI backplane on the listed J3 pins.

A.8 PCI Mezzanine Card (PMC2) Connectors (JN1 & JN2)

This section has the pin-outs for both of the PMC connectors for the second PMC site, labeled PMC2 at the front panel. Connectors JN1 & JN2 are labeled as P21 and P22 resepctively.

Pin	Signal	Pin	Signal
1	5.6K pull-down	2	-12 VDC
3	GND	4	INTF#
5	INTG#	6	INTH#
7	No connection	8	+5 VDC
9	INTE#	10	No connection
11	GND	12	No connection
13	PCI CLK	14	GND
15	GND	16	GNT0#
17	REQ0#	18	+5 VDC
19	VI/O	20	AD31
21	AD28	22	AD27
23	AD25	24	GND
25	GND	26	C/BE3#
27	AD22	28	AD21
29	AD19	30	+5 VDC
31	VI/O	32	AD17
33	FRAME#	34	GND
35	GND	36	IRDY#
37	DEVSEL#	38	+5 VDC
39	PCIXCAP (grounded)	40	LOCK#
41	No connection	42	No connection
43	PAR	44	GND
45	VI/O	46	AD15
47	AD12	48	AD11
49	AD9	50	+5 VDC
51	GND	52	C/BE0#
53	AD6	54	AD5
55	AD4	56	GND
57	VI/O	58	AD3
59	AD2	60	AD1
61	AD0	62	+5 VDC
63	GND	64	REQ64#

PCI Mezzanine Card (PMC2) Connector (P21) – Molex 71439-0164

VIO is jumper selectable (through JP3, please see Section 4.1).

Pin	Signal	Pin	Signal
1	+12 VDC	2	TRST (pulled down)
3	TMS (pulled up)	4	No connection
5	TDI (pulled up)	6	GND
7	GND	8	No connection
9	No connection	10	No connection
11	+3.3 VDC	12	+3.3 VDC
13	PCI RST#	14	GND
15	+3.3 VDC	16	GND
17	No connection	18	GND
19	AD30	20	AD29
21	GND	22	AD26
23	AD24	24	+3.3 VDC
25	AD16 (IDSEL)	26	AD23
27	+3.3 VDC	28	AD20
29	AD18	30	GND
31	AD16	32	C/BE2#
33	GND	34	No connection
35	TRDY#	36	+3.3 VDC
37	GND	38	STOP#
39	PERR#	40	GND
41	+3.3 VDC	42	SERR#
43	C/BE1#	44	GND
45	AD14	46	AD13
47	M66EN	48	AD10
49	AD8	50	+3.3 VDC
51	AD7	52	No connection
53	+3.3 VDC	54	No connection
55	No connection	56	GND
57	No connection	58	No connection
59	GND	60	No connection
61	ACK64#	62	+3.3 VDC
63	GND	64	No connection

PCI Mezzanine Card (PMC2) Connector (P22) – Molex 71439-0164

B. Address Maps, Interrupts, DMA Channels

Tables of the CPM1's address maps, interrupt request assignments, and DMA channel usage are given in the following sections. All addresses are shown in hexadecimal notation.

B.1 Memory Map

The CPM1's memory map is shown below:

Address Range	Description
00000000 – 000FFFFF	DOS legacy address range
00100000 - Top of On-board DDR SDRAM Memory	On-board DDR DRAM 1GB
Top of On-board DRAM Memory – FEBFFFFF	PCI Device Allocation
FEC00000 - FEEFFFFF	APIC Configuration Area (unused on CPM1)
FFE00000 - FFFFFFFF	High BIOS Area

This is the memory map on the GMCH.

For further details on the CPM1 memory space map, refer to Section 5.1 in *Intel's 855GM/855GME Chipset Graphics and Memory Controller Hub(GMCH) Datasheet*, Document # 252615-004, available from Intel Corporation.

B.2 PCI Configuration Space Map

The PCI configuration space map will vary if the PMCX expansion slot is used to support a PMCX add-on mezzanine card and if that PMCX module uses a expansion bridge designed for multiple targets on the secondary bus. This is an extremely unlikely situation but the bus numbers in this condition will differ from those provided in the following table. The Vendor ID and Device ID in hex for the PMCX slot are shown as *xxxx*, since they depend on the type of device installed in the PMC slot.

IDSEL	Bus	Dev	Fcn	VenID	DevID	Description
—	00	30	0	8086	244E	6300ESB (ICH) P2P Bridge
—	00	31	0	8086	25A1	6300ESB (ICH) P2L Bridge
—	00	31	1	8086	25A2	6300ESB (ICH) PCI-IDE Interface
—	00	31	2	8086	25A3	6300ESB (ICH) SATA Interface
—	00	31	3	8086	25A4	6300ESB (ICH) SMBus Interface
—	00	29	0	8086	25A9	6300ESB (ICH) PCI-USB#0 Interface
—	00	29	1	8086	25AA	6300ESB (ICH) PCI-USB#1 Interface
—	00	29	5	8086	25AC	6300ESB (ICH) APIC
AD16	03	0	0	8086	1229	82541 Fast Ethernet Controller
AD17	03	1	0	10E3	0000	PCI 6254PCI-cPCI Interface
AD18	02	2	0	8086	1010	82546 Gb Ethernet Channel #1
—	00	2	0	8086	3582	GMCH-integrated Graphics Controller
AD17	02	1	0	xxxx	xxxx	PMCX Site for an Add-on Mezzanine Card

PCI Configuration

B.3 Interrupt Request Routing

The ISA interrupt request routing is shown below:

IRQ	Description
0	Timer 0 (ICH)
1	Keyboard (SMSC's LPC47B272*)
2	Cascade Interrupt from slave PIC (ICH)
3	COM2/COM4 (LPC47B272)
4	COM1/COM3 (LPC47B272)
5	LPT2 (LPC47B272)
6	Floppy Drive (LPC47B272)
*7	LPT1 (LPC47B272)
8	Real Time Clock (ICH)
9	No connection (pulled up via 8.2K)
10	No connection (pulled up via 8.2K)
11	No connection (pulled up via 8.2K)
12	Mouse (LPC47B272's kybd/mouse controller)
13	Math Coprocessor (ICH)
14	Primary IDE Interface via P2 connector (ICH)
15	Secondary IDE Interface (CompactFlash) (ICH)

*The LPC47B272 is found on the optional CPM1PTB rear I/O expansion card, it is not included with the CPM1.

The PCI interrupt request routing to the Intel 6300ESB I/O Controller Hub (ICH) is shown below:

PIIX4 PCI IRQ	Description
PIRQA#	USB 0
*PIRQB#	82546EB
PIRQC#	GMCH-integrated SVGA Controller
*PIRQD#	USB 1, PCI 6254LINT0#

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For further details on interrupts, refer to the documentation for the various peripherals that generate interrupts, as well as *Intel 6300ESB I/O Controller Hub Datasheet*, Document #300641-002.

C. Power and Environmental Requirements

The CPM1 power and environmental requirements are shown in the tables below.

Condition	Power Requirements
1.4 MHz Pentium M	5 VDC @ 2.0 A typ., 3.3 VDC @ 2.0 A typ 3.0 VDC Lithium Coin Cell @ 3.4 µA

Power Requirements

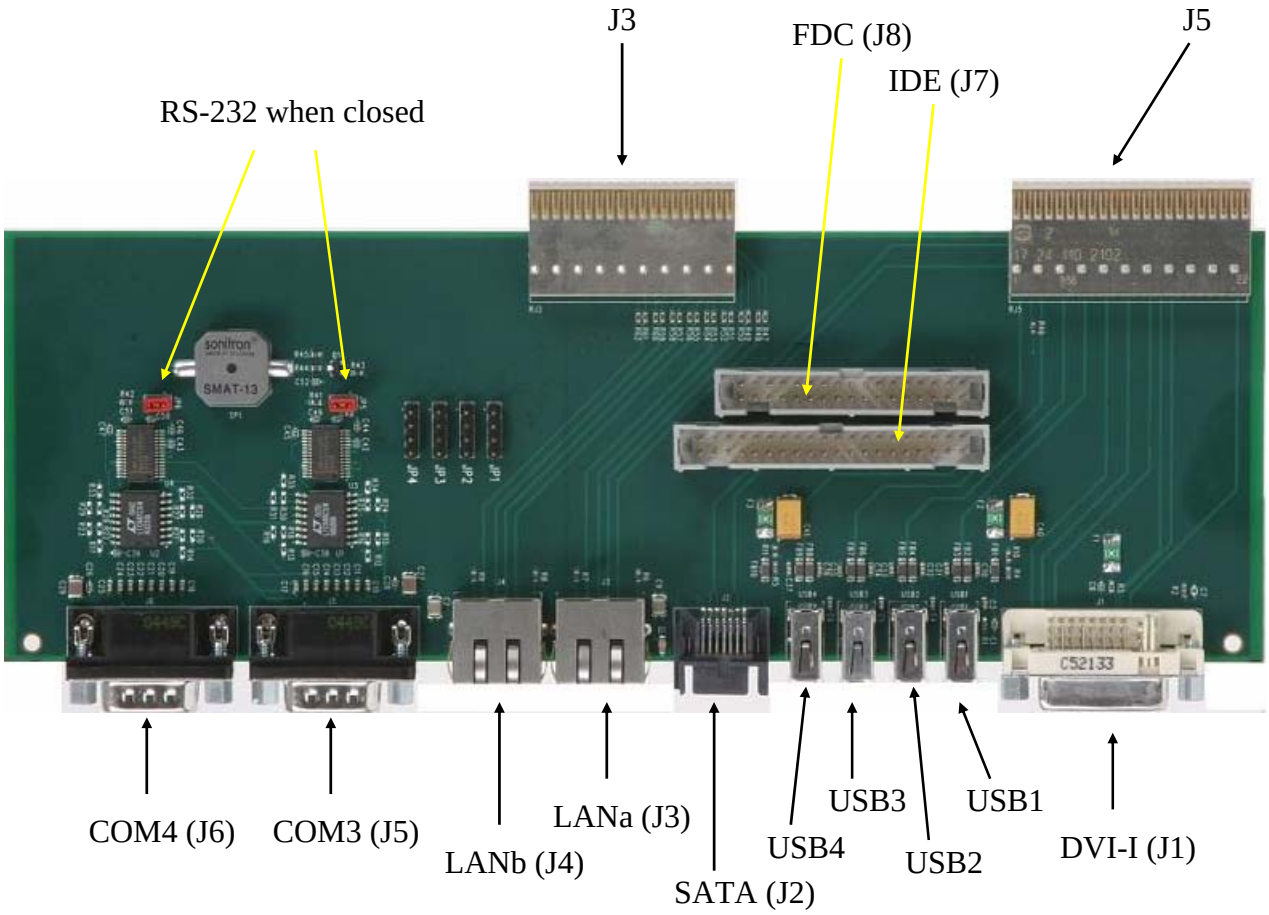
The 3 Volt lithium coin cell is a CR2032 with 190 mAhours capacity and it is used to battery-back the Real Time Clock, the 2 MB of NV-SRAM, and the BIOS's NV-RAM. At 3.4 µA this battery should last for over six years with power off.

Condition	Environmental Requirements
Operating Temperature	-40° to +71° C
Storage Temperature	-50° to +105° C

Environmental Requirements

D. XPM1RIO Rear Plug-in I/O Expansion Module for the CPM1

Much of the CPM1's I/O is driven directly through the J3 and J5 connectors so a rear plug-in module is useful for interfacing to industry standard cables. The XPM1RIO is available for this purpose. Here is a photo of the XPM1RIO:



Fan Connectors