DMC VMEbus Pentium III Based Dual PMC Module Carrier Board

User's Manual

DMC User’s Manual Rev. 1.00

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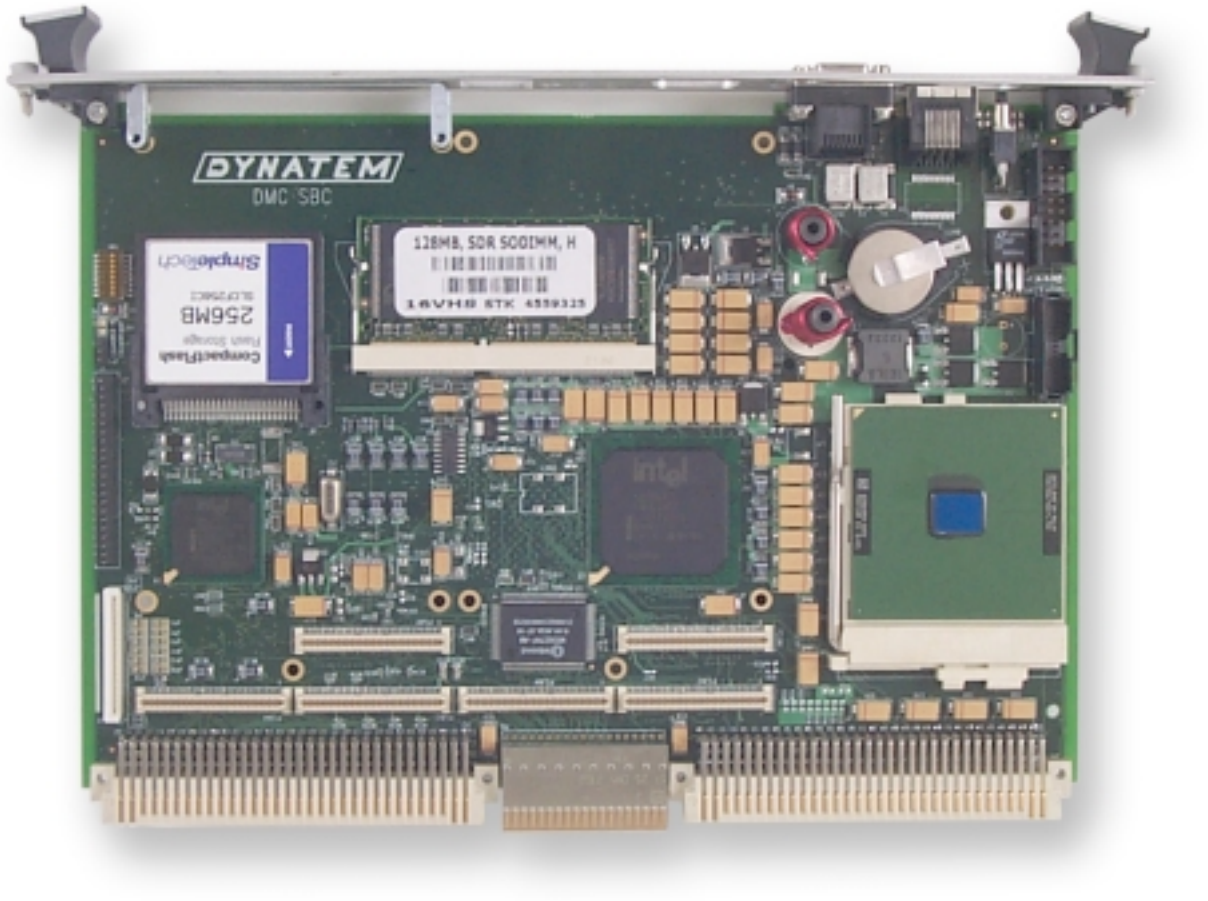
1. Features

The Dynatem DMC is a single-slot 6U VMEbus Single Board Computer (SBC). The DMC offers full PC performance with a Socket 370 processor and it also offer two Fast Ethernet ports and two PMC sites for greater expansion capability.



The DMC employs Intel's embedded technology to assure long-term availability. The Socket 370 processor will track commercial product, however, for low cost and high performance.

Features of the DMC include:

- Single-slot VMEbus operation with on-board CompactFlash disk for bootable mass storage and front panel connectors for Keyboard/Mouse, VGA, and 10/100BaseTX
- COM1/2, LPT1, PMC I/O, mouse/keyboard, a second 100BaseTX port, USB, Soundblaster, Game Port, IDE and FDC are routed out to the backplane via a five-row VME64 P2 connector and a P0 connector
- Socket 370 supports readily available processors from an 850 MHz Celeron to a 1.4 MHz Tualatin Pentium III

- High-performance Intel 815E chipset with DRAM controller, PCI bus arbitration logic and interface, built-in video interface, Ultra ATA IDE interface, USB interface, RTC, NV-RAM, standard PC timers, and interrupt logic.
- An SO-DIMM socket supports up to 512 MB of SDRAM at 133 MHz
- Tundra Universe IID PCI-VMEbus Interface provides 64-bit VMEbus transfer rates over 30 MB/sec. Integral FIFOs permit write-posting to maximize available PCI and VMEbus bandwidth. Full Slot 1 (System Controller) functionality is provided
- Two Intel's 82559 Fast Ethernet Controllers with 10/100BaseTX support
- Two PCI Mezzanine Cards (PMC) are supported with front panel I/O, while maintaining VMEbus single-slot form factor
- Primary Ultra DMA IDE Interface with improved transfer rates and PIO and Bus Master support
- Secondary IDE port for CompactFlash on-board booting for flash-based and mechanical storage
- General Software's flash-based system BIOS
- Floppy drive controller with support for drives of up to 2.88 MB
- COM1 and COM2 serial ports, based on 16C550 compatible UARTs with 16-byte transmit and receive FIFOs
- LPT1 parallel port that's capable of standard, bidirectional, enhanced parallel port (EPP), and enhanced capabilities port (ECP) operation, with IEEE 1284 compliance.
- Programmable watchdog timer for system recovery.
- Operating System (OS) and driver support, including Windows NT, Embedded NT, QNX, VxWorks, Linux, Solaris, and pSOS+.

2. Related Documents

Listed below are documents that describe the Pentium processor and chipset, and the peripheral components used on the DMC. Contact your local distributor for copies of these documents.

For a data sheet on the Pentium III, go to:

http://developer.intel.com/design/intarch/pentiumiii/pentiumiii.htm

For a data sheet on the Celeron, go to:

http://developer.intel.com/design/intarch/celeron/celeron.htm

For Intel data, go to:

http://developer.intel.com/design/litcentr/index.htm

The Intel website is subject to change but the following documents should be available and downloadable:

- *Pentium ® III Processor for the PGA370 Socket at 500 MHz to 1.13 GHz*
  ftp://download.intel.com/design/PentiumIII/datashts/24526408.pdf

- *Intel ® Celeron ® Processor for the PGA370 Socket up to 1.40 GHz on 0.13 Micron Proces*
  ftp://download.intel.com/design/celeron/datashts/29859604.pdf

- *Intel ® 82801BA I/O ControllerHub 2 (ICH2) and Intel ® 82801BAMI/O Controller Hub 2 Mobile(ICH2-M)*
  http://developer.intel.com/design/chipsets/datashts/290687.htm

- *Intel Chipset Family: 82815 Graphics and Memory ControllerHub (GMCH)*
  ftp://download.intel.com/design/chipsets/datashts/29068801.pdf

- *82559ER Fast Ethernet PCI Controller*
  http://developer.intel.com/design/network/products/lan/controllers/82559er.htm

- *VMEbus Interface Components Manual*
  Tundra Semiconductor Corporation; Universe IID revisions are found at www.tundra.com

- *Winbond W83627HF/F Super I/O Device Data Sheet*
  Winbond's website is http://www.winbond.com.tw/e-winbondhtm/index.asp

- The following documents provide information on the PC architecture:

- *PCI Local Bus Specification, Revision 2.1*
  PCI Special Interest Group

The following documents cover topics relevant to the VMEbus and can be purchased through VITA:

- IEEE Std 1014-1987, *IEEE Standard for a Versatile Backplane Bus: VMEbus*
  The Institute of Electrical and Electronic Engineers
  345 East 47th Street
  New York, NY 10017
  (800) 678-4333

- Wade D. Peterson, *The VMEbus Handbook*
  VITA
  10229 North Scottsdale Road, Suite B
  Scottsdale, AZ 85253
  (480) 951-8866

The following documents are the current draft standards for the PCI Mezzanine Card (PMC):

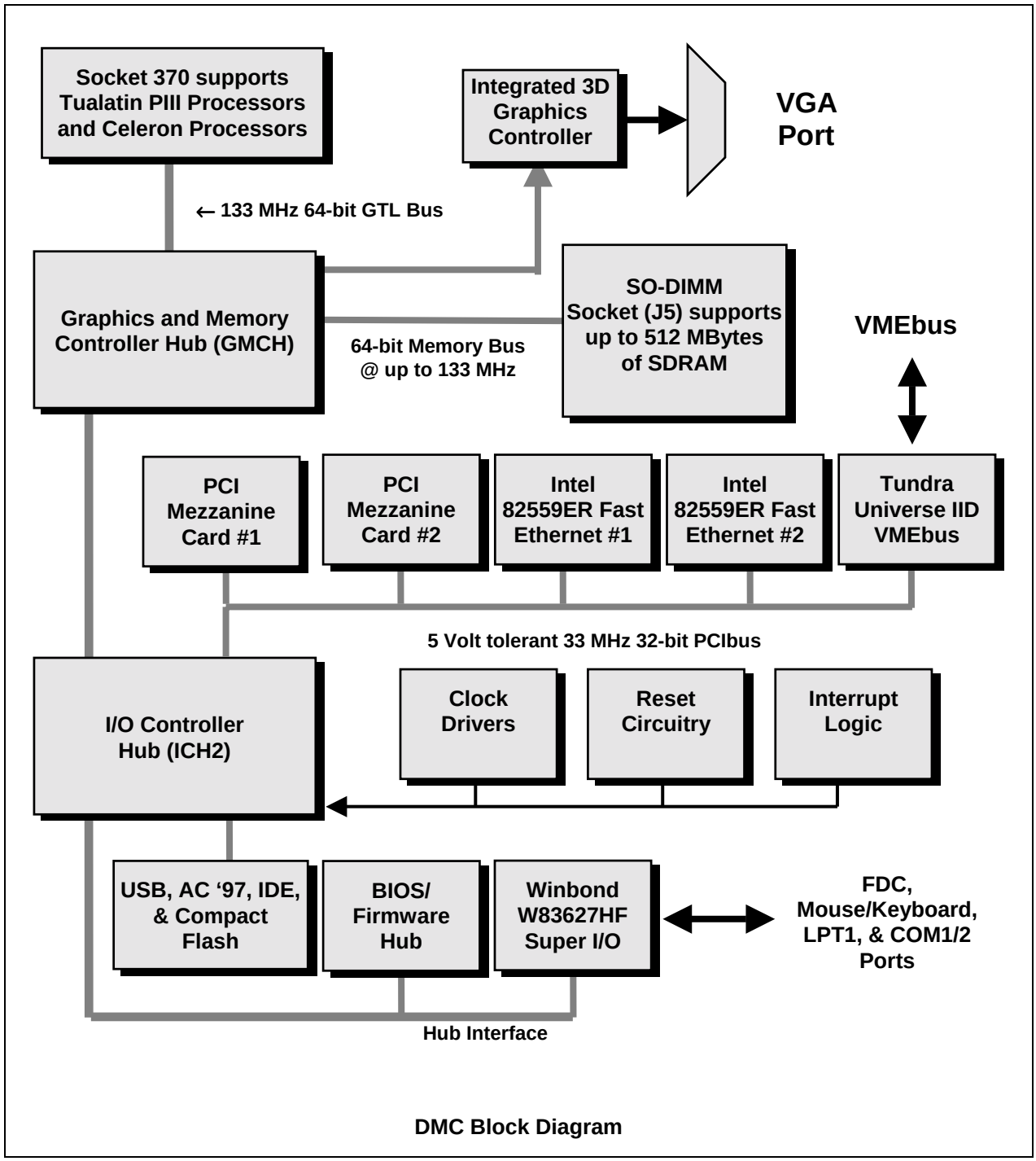
- IEEE Draft Std P1386/2.0, *Draft Standard for a Common Mezzanine Card Family: CMC*
  The Institute of Electrical and Electronic Engineers
  345 East 47th Street
  New York, NY 10017
  (800) 678-4333

- IEEE Draft Std P1386.1/2.0, *Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC*
  The Institute of Electrical and Electronic Engineers
  345 East 47th Street
  New York, NY 10017
  (800) 678-4333

3. Hardware Description

3.1 Overview

The block diagram of the DMC is shown below. The sections that follow describe the major functional blocks of the DMC.



DMC Block Diagram

3.2 Processor

The DMC supports a Socket 370 processor. Both Tualatin Pentium III's and Celeron processors are supported.

- Processor System Bus (PSB) of up to 133 MHz.
- Built-in Level 1 instruction (code) and data caches of 16 KB each and up to 512 KB of on-die L2 cache.
- Integrated math co-processor.
- Power management, MMX, and backwards compatibility with Pentium class processors.

For further information on the Pentium processor, refer to *Pentium Processors and Related Products*, available from Intel Corporation.

3.3 Intel 815E Chipset

With the 2nd generation I/O Controller Hub (ICH2), the Intel® 815E chipset offers greater platform flexibility and stability in Celeron® and Pentium® III processor-based PCs. The Intel 815E chipset consists of two devices: Graphics and Memory Controller Hub (GMCH) and the I/O Controller Hub (ICH2). The GMCH integrates the following functions into a single ball-grid array (BGA) package:

- Built-in graphics accelerator which supports VGA resolutions up to 1600 x 1200.
- 133 MHz DRAM controller supporting up to 512 MB of Synchronous DRAM (SDRAM) which are accessed from an on-board SO-DIMM connector.
- 133 MHz 64 bit front side processor bus.

The ICH2 integrates the following functions into a single ball-grid array (BGA) package:

- PCI 2.2 compliant, high-performance Processor-to-PCI buffered bridge with PCI bus arbitration logic.
- USB support and AC'97 2.1 compliant link for audio and telephony codecs.
- Primary and secondary Ultra ATA/100/66/33 interfaces. The IDE signals are brought out to J7 and J6. The primary IDE port, J7, is a 44-pin dual-row 2-mm header on the PCB. The secondary port, J6, is a CompactFlash Type II connector. The pin-outs for these connectors are given in Appendix A.
- Enhanced DMA controller, interrupt controller, and timer functions.

For further information, see the documents referenced in Section 2.

3.4 DRAM

The DMC supports up to 512 MB of Synchronous DRAM (SDRAM) with a 144-pin SO-DIMM socket for additional 3.3 V PC100 SDRAM memory. When a processor with a front side bus of 133 MHz is populated in the DMC's socket 370, SO-DIMM's compliant with PC133 (133 MHz transfer rates) may be installed. Jumpers JP1 and JP2 determine the frequency of the front side bus and the SO-DIMM's DRAM interface.

The SO-DIMM socket is J5 and it is located beneath the two PMC modules. While these SO-DIMM's are industry standard, we recommend ordering this DRAM from Dynatem as it will be tested at the factory for electronic and mechanical compatibility.

3.5 Intel 82559 Fast Ethernet Controller

The DMC provides two 82559 Fast Ethernet controllers. The Intel 82559 offers the following features:

- 10BaseT and 100BaseTX support with auto-negotiation.
- Independent 3 KB receive and transmit FIFOs.
- Powerful on-chip DMA minimizes CPU overhead with zero wait-state burst transfers to system memory.
- Built-in Phyceiver.
- Serial EEPROM for nonvolatile Ethernet address storage.

The 10BaseT/100BaseTX signals of one of the 82559 controllers are brought out to J1, an RJ-45 connector on the front panel. The pin-out for J1 is given in Appendix A. Three front panel LEDs are located below the front panel reset button and are controlled by the Ethernet circuitry: CR1 is closest to the RJ-45 connector (it is on when transferring at 100 Mb/sec, off when transferring at 10 Mb/sec), CR2 (active) is positioned next, and CR3 (link established) is the last indicator LED for the first Ethernet port.

The DMC's second 82559 has its I/O lines routed to VMEbus connector P2. Both Dynatem's rear I/O breakout card (model XMCPTB) and the 2nd-slot mass storage transition module (model XMCTB) run these lines through a transformer and out an RJ-45 connector. Indicator LED's for the second LAN port are located next to those for the first port, below the reset button. These three LED's follow the same pattern as those for the first port.

The Intel 82559 contains several PCI configuration registers. It also contains a number of device registers for controlling the Ethernet operation that can be mapped to the memory space or the I/O space. The PCI signals specific to the DMC's first 82559 are shown below:

Intel 82559 Signal	PCI Bus Connection
IDSEL	AD23 (PCI Device 0Ch)
PREQ	REQ2# (ICH2)
PGNT	GNT2# (ICH2)
PIRQ	PIRQH# (ICH2)

The PCI signals specific to the DMC's second 82559 are shown below:

Intel 82559 Signal	PCI Bus Connection
IDSEL	AD24 (PCI Device 0Ch)
PREQ	REQ3# (ICH2)
PGNT	GNT3# (ICH2)
PIRQ	PIRQG# (ICH2)

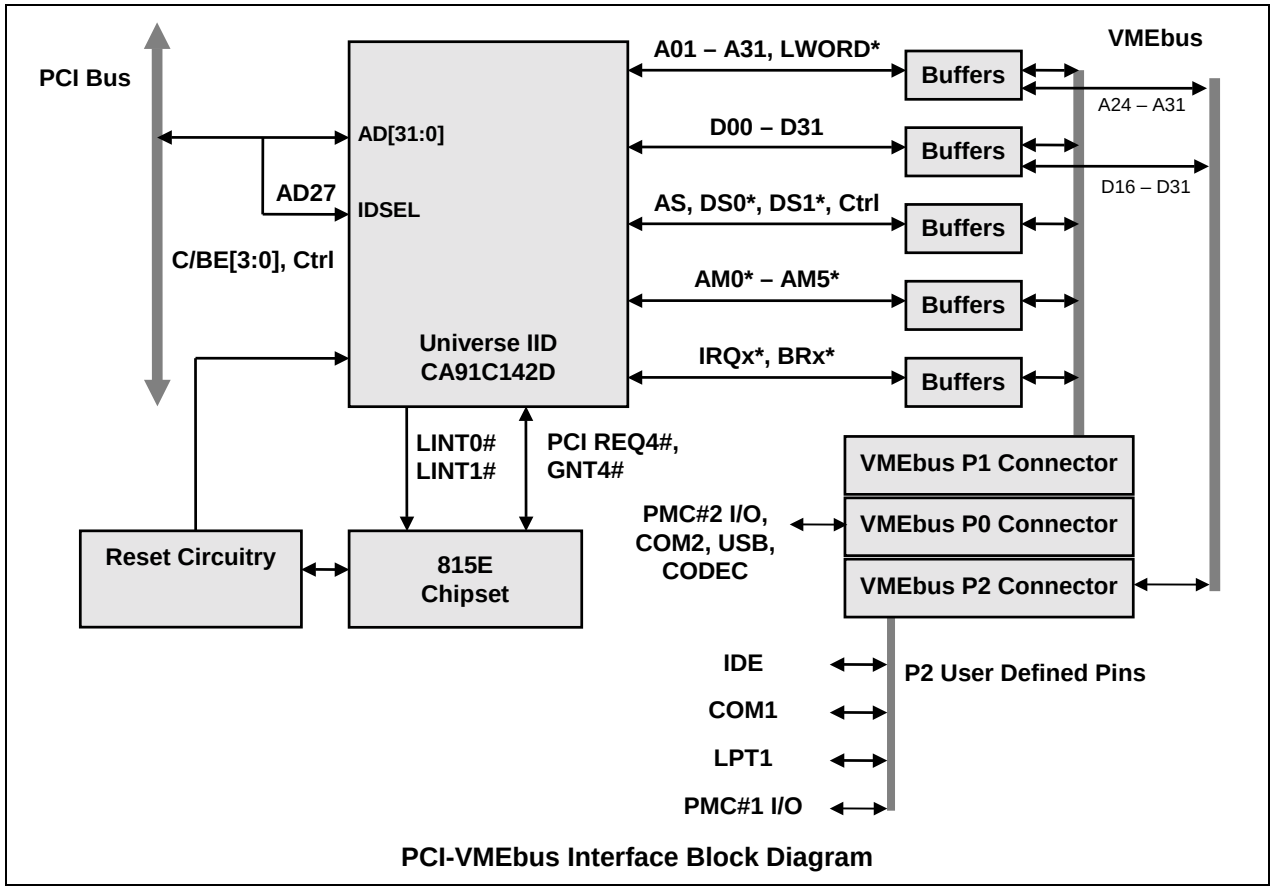
For further information on the 82559, refer to *82559 Fast Ethernet Multifunction PCI/Cardbus Controller*, available from Intel Corporation. Please go to the link at:
http://developer.intel.com/design/network/products/lan/controllers/82559.htm

3.6 Tundra Universe IID CA91C142D PCI-VMEbus Interface

The PCI-VMEbus interface, based on the Tundra Universe IID CA91C142D, offers the following features:

- High-performance 64-bit VMEbus interface.
- Integral FIFOs for write-posting allow the Universe IID to quickly relinquish the bus.
- Programmable DMA controller with linked list support.
- Full VMEbus system controller functionality.
- Complete VMEbus address and data transfer modes:
    - A32/A24/A16 master and slave
    - D64 (MBLT)/D32/D16/D08 master and slave
- Flexible register set, programmable from both the PCI bus and the VMEbus.

The block diagram of the PCI-VMEbus interface is shown below:



PCI-VMEbus Interface Block Diagram

As shown in the block diagram, several peripheral signals are routed to the user-defined pins of the VMEbus P2 connector. The VMEbus P1 and P2 connector pin-outs are given in Appendix A.

The Universe IID CA91C142D can act as a PCI bus initiator (master) or target (slave), and a VMEbus master or slave. The Universe IID is capable of generating interrupts on the VMEbus, and can act as a VMEbus interrupt handler. The Universe IID provides full VMEbus system controller functionality. The DMC reset circuitry is tied to the Universe IID, since the DMC can generate the VMEbus SYSRESET* signal as well as be reset by another VMEbus board that asserts the SYSRESET* signal. The DMC reset circuitry is discussed in detail in Section 3.12.

This section is intended to supplement the VME-to-PCI Bus Bridge Manual User Manual (downloadable from www.tundra.com), which contains comprehensive descriptions of the operation and programming of the Universe IID. In that manual, Chapter 1, *Functional Overview*, Chapter 5, *Registers Overview*, and Chapter 12, *Registers*, provide the necessary information to understand the operating modes of the Universe IID:

- DMC-initiated transfers (PCI slave, VMEbus master).
- Other VMEbus master-initiated transfers (PCI master, VMEbus slave).
- DMA controller transfers (PCI master, VMEbus master).
- VMEbus interrupt generation.
- VMEbus interrupt handling.
- System controller functionality.
- Register programming via the PCI bus and the VMEbus.
- Coupled and uncoupled transfers between the PCI bus and the VMEbus.
- 4 mailboxes and 8 semaphores.
- VMEbus arbitration.

The Universe IID Control and Status Registers (UCSRs) are used for the configuration of the Universe IID. These registers form a 4 KB block, divided into three groups:

- PCI Configuration Space (PCICS).
- Universe IID Device Specific Status Registers (UDSRs).
- VMEbus Control and Status Registers (VCSRs).

These registers are accessible (to varying degrees) via three address spaces:

- PCI Configuration Space – Only the PCICS register block is accessible in this space.
- PCI Memory Space – The entire 4 KB UCSR block is accessible in this space.
- VMEbus A32/A24/A16 Space – The entire 4 KB UCSR block is accessible in this space.

During initialization, the system BIOS maps PCI peripherals that require space beyond the PCI configuration space into the memory space or I/O space. The Universe IID UCSR block is 4 KB in size and must be aligned on a 64 KB boundary. The total I/O space of an Intel processor is 64 KB and many of the common PC peripherals are found in the first 1 KB of this space. Thus, a request for a 64 KB block of I/O space for the Universe IID registers would be denied by the system BIOS, leaving the Universe IID unmapped. To avoid this situation, the Universe IID offers a power-up option to map its registers into the memory space. This is accomplished on the DMC by tying the VA[1] line high via a pull-up resistor.

There are two mechanisms to access the UCSR block from the VMEbus. The first is the VMEbus Register Access Image (VRAI) method, which is defined by the following registers in the Universe IID *User's Manual*:

Field	Register Bits	Description
Address Space	VAS in Table A.76	A32, A24, or A16
Base Address	BS[31:12] in Table A.77	Lowest address in the 4 KB slave image
Slave Image Enable	EN in Table A.76	Enable VMEbus Register Access Image
Mode	SUPER in Table A.76	Supervisor and/or Non-Privileged
Type	PGM in Table A.76	Program and/or Data

The reset state of the VAS, BS[31:12], and EN fields can be configured as power-up options. On the DMC, all of these fields reset to 0. Thus, the VRAI method must be configured and enabled by accessing the Universe IID registers in the memory space.

The second mechanism for accessing the UCSR block from the VMEbus is the CS/CSR method, which is defined by the following registers in the Universe IID section of the *User's Manual*:

Field	Register Bits	Description
Base Address	BS[23:19] in Table A.84	Base address of Universe IID 512 KB slot
Slave Image Enable	EN in Table A.78	Enable CS/CSR image

The BS[23:19] and EN fields reset to all 0s, and the EN bit can be set by the VME64 Auto ID process. Thus, the CR/CSR method must be configured by accessing the Universe IID registers in the memory space.

The PCI signals specific to the Tundra Universe IID CA91C142D are shown below:

Tundra Universe IID CA91C142D Signal	PCI Bus Connection
IDSEL	AD27 (PCI Device 10h)
REQ#	REQ4# (ICH2)
GNT#	GNT4# (ICH2)
LINT0#	PIRQG# (ICH2)
LINT1#	EXTSMI# (ICH2)

3.7 PCI Mezzanine Card (PMC) Slots

The DMC offers two PCI Mezzanine Card (PMC) sites for more flexible I/O expansion. The first PMC site (designated PMC #1) is closer to the Socket 370 processor and its heat sink. The PMC Slot offers the following characteristics:

- Conforms to IEEE draft standards 1386/2.0 and 1386.1/2.0.
- Accepts single-width 5V PMC boards with front panel I/O as well as backplane I/O.
- Provides 32-bit PCI support via connectors JN1 and JN2, and JN4 is available for routing PMC I/O to VMEbus connector P2. The two PMC sites do not offer JN3 connectors for 64-bit PCI support, but cards containing a PN3 connector are accommodated (that is, no components on the DMC interfere with a PMC PN3 connector).

The PCI signals specific to the two PMC Slots are shown below:

PMC #1 Slot Signal	PCI Bus Connection
IDSEL	AD16 (PCI Device 0Fh)
REQ#	REQ0# (ICH2)
GNT#	GNT0# (ICH2)
PMCINTA#	PIRQA# (ICH2)
PMCINTB#	PIRQB# (ICH2)
PMCINTC#	PIRQC# (ICH2)
PMCINTD#	PIRQD# (ICH2)

PMC #2 Slot Signal	PCI Bus Connection
IDSEL	AD17 (PCI Device 0Fh)
REQ#	REQ1# (ICH2)
GNT#	GNT1# (ICH2)
PMCINTA#	PIRQB# (ICH2)
PMCINTB#	PIRQC# (ICH2)
PMCINTC#	PIRQD# (ICH2)
PMCINTD#	PIRQA# (ICH2)

The DMC routes most of the JN4 I/O pins of the two PMC sites to the VMEbus backplane. With PMC #1, pins 1 through 46 of its JN4 I/O connector are routed to the P2 VMEbus connector. With PMC #2, pins 1 through 60 of its JN4 I/O connector are routed to the P0 VMEbus connector. Depending on whether the integrator's I/O will be routed to the backplane, on how many of those JN4 I/O pins are needed, and whether a VME64 Extensions backplane (with P0 support) is used, care should be taken regarding site assignment. Appendix A has the pinouts for VMEbus backplane connectors P0 and P2.

For further information on the PMC specification, refer to *PCI Local Bus Specification, Revision 2.2*, available from the PCI Special Interest Group (www.pcisig.com), IEEE Draft Std P1386-2001, *IEEE Standard for a Common Mezzanine Card Family: CMC*, and IEEE Draft Std P1386.1-2001, *IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC*, both available from the Institute of Electrical and Electronic Engineers.

3.8 Winbond W83627HF/F Super I/O Device

The Winbond W83627HF/F provides the following standard PC peripherals:

- Floppy drive controller with support for drives up to 2.88 MB with a 2Mbps transfer rate.
- COM1 and COM2 serial ports, based on 16C550 compatible UARTs with 16-byte transmit and receive FIFOs.
- LPT1 parallel port that's capable of standard, bidirectional, enhanced parallel port (EPP), and enhanced capabilities port (ECP) operation, with IEEE 1284 compliance.
- Infrared port that supports IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps

The W83627HF/F clock input is driven by a 24 MHz clock and it uses the Low Pin Count (LPC) interface with the 815E chipset. The COM1 and LPT1 signals are routed to the user defined pins of the VMEbus P2 connector. The floppy drive signals are routed to J8, a 1.00mm ZIF flex circuit connector on the PCB and they can optionally be routed to P2 when jumpers JP5 through JP16 are closed. The COM2, CODEC, Joystick, and IR signals are brought out to VMEbus connector P0. The connector pin-outs are given in Appendix A.

The Winbond W83627HF I/O space addresses upon power-up or reset are shown below:

Winbond W83627HF/F	I/O Address
Configuration	3F0, 3F1
COM1	3F8 - 3FF
COM2	2F8 - 2FF
Parallel Port	278 - 27F
Floppy Drive Interface	3F0 - 3F7

The W83627HF defaults to LPT2 (278-27F) upon power-up or reset, but the system BIOS can reconfigure the parallel port for operation as LPT1 (378-37F), LPT2 (278-27F), or LPT3 (3BC-3BF). Thus, throughout this manual the parallel port is referred to as LPT1.

The Winbond W83627HF interrupt request line assignments are shown below:

Winbond W83627HF/F Function	Interrupt Request Line
COM2, COM4	IRQ3
COM1, COM3	IRQ4
LPT2	IRQ5
Floppy	IRQ6
LPT1	IRQ7

The Winbond W83627HF DMA channel assignments are shown below:

Winbond W83627HF/F Function	DMA Channel
Floppy	DMA Channel 2
Parallel Port (ECP mode)	DMA Channel 5

The keyboard/mouse controller, based on the Intel 8042, is built-in to the W83627HF and it is a standard 8-bit ISA peripheral for controlling a PS/2 style keyboard and a PS/2 style mouse. Power is supplied to the keyboard and mouse via a 1 amp self-resetting fuse (F1). The keyboard and mouse signals are routed to J2-2, which is a 6-pin mini-DIN receptacle on the front panel. The pin-out of J2-2 is given in Appendix A.

The W83627HF's keyboard/mouse controller I/O space addresses are shown below:

W83627HF's Keyboard/Mouse Controller Register	I/O Address
Keyboard/Mouse Data	60
Keyboard/Mouse Status/Command	64

The W83627HF's keyboard/mouse controller interrupt request line assignments are shown below:

W83627HF's Keyboard/Mouse Controller Function	Interrupt Request Line
Keyboard Buffer Full	IRQ1
Mouse Buffer Full	IRQ12

For further information on the W83627HF, refer to the *W83627HF Data Sheet,* available from Winbond, their website is at http://www.winbond.com.tw/e-winbondhtm/index.asp

3.9 Real Time Clock and NVRAM

Both the Real Time Clock (RTC) and the NVRAM for holding battery-backed BIOS parameters are contained within the FW82801BA I/O Controller Hub 2 (ICH2). The RTC generates IRQ8. NVRAM addresses use I/O address 70 while NVRAM data use I/O address 71. The ICH2 is battery-backed by an on-board lithium coin cell.

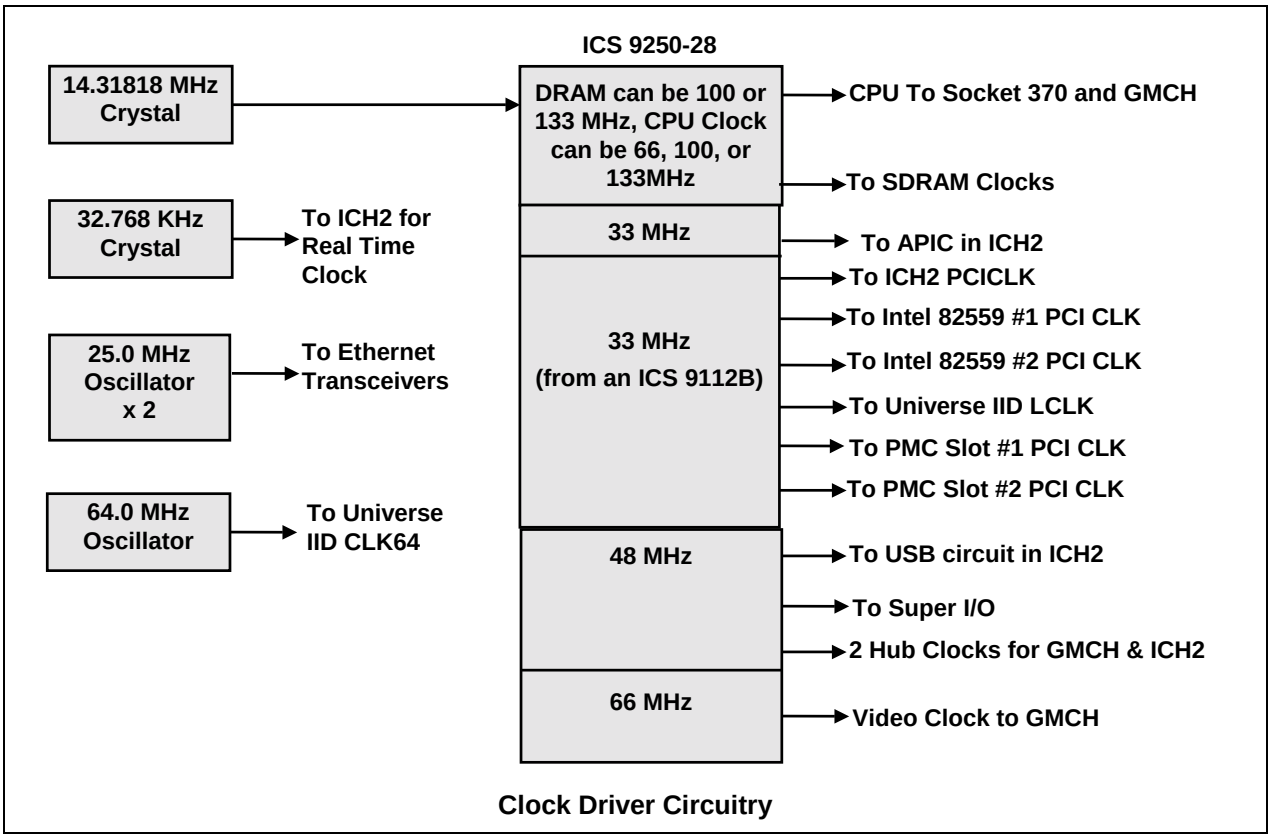
3.10 Intel's E82802AC Firmware Hub

The Intel E82802AC uses a 5-pin interface and provides 8 Mb of flash memory for the system BIOS. This device can fill the 1 MB real mode memory map so only a portion, the upper 256 MB, is used. The E82802AC's 1 MB of memory space is segmented into sixteen parameter blocks of 64 KB each. The DMC powers up into real mode and the BIOS is eventually shadowed into system DRAM after booting through the BIOS. Here is how the ICH2 chip maps the real mode:

The FW82801BA (ICH2) provides the 5-pin interface to the E82802AC. The upper 256 KB of the E82802AC is located from 000C0000 - 000FFFFF (the top of 1 MB) and its full 1 MB of memory is aliased from FFF00000 – FFFFFFFF where it can be fully accessed after booting up through the BIOS.

3.11 Clock Drivers

The clock driver circuitry is shown below:



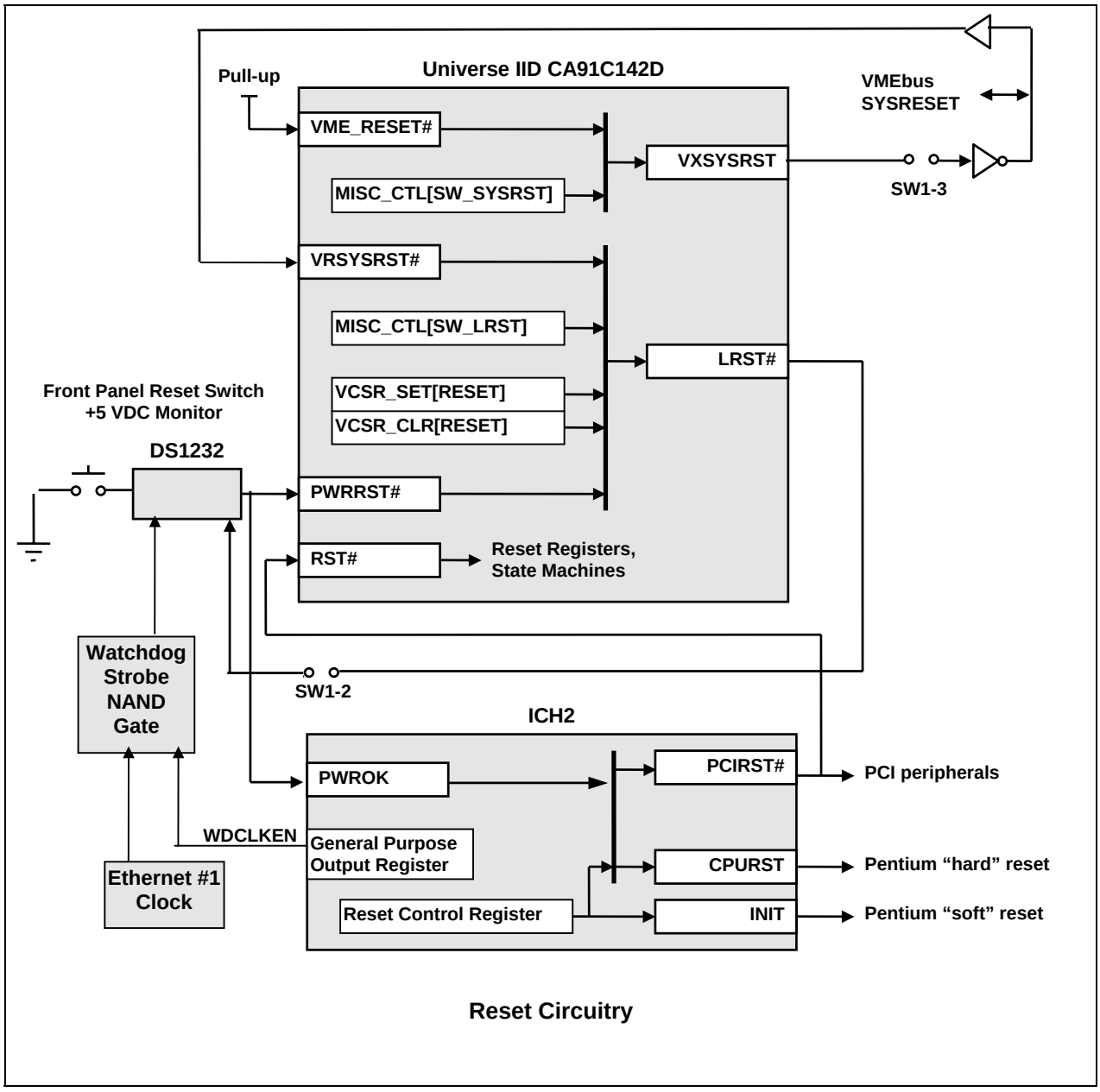
Clock Driver Circuitry

The clock driver circuitry is based on the ICS 9250 and the ICS 9112B (the 9112B is used to generate multiple PCI clocks at 33 MHz), driven by a 14.31818 MHz crystal. A 32.768 KHz Crystal drives the Real Time Clock (RTC) to the ICH2, two separate 25.0 MHz oscillators drive the two Ethernet ports, and a 64.0 MHz oscillator drives the Universe IID CA91C142D VMEbus circuitry.

The CPU and DRAM clocks, as indicated in the drawing above, are configurable. Jumpers JP1 & JP2 determine these clock rates.

3.12 Reset Circuitry

The reset circuitry is shown below:



Reset Circuitry

Opening SW1-3 will prevent the DMC's hard reset from resetting the VMEbus backplane (see next page). Opening SW1-2 will isolate the DMC from VMEbus SYSRESETs. **Either SW1-3 or SW1-2 should be closed – <u>but never both at the same time</u>.**

There are eight ways to perform a hard reset of the DMC:

- The DS1232 senses that the +5 VDC supply has dropped too low, which asserts a PWROK signal to the ICH2, the Super I/O, and to the Universe IID. This signal resets the processor and the Chipset and, ultimately, all PCI peripherals.

- The front panel reset switch is pressed, which also asserts a PWROK signal and resets the DMC.

- Another VMEbus board asserts SYSRESET*, which asserts the Universe IID VRSYSRST# input and, if switch SW1-2 is closed, will reset the DMC via the DS1232.

- The SW_SYSRST bit in the MISC_CTL register of the Universe IID is set by code running on the DMC processor. This leads to the assertion of the VMEbus SYSRESET* signal, if SW1-3 is closed.

- The SW_LRST bit in the MISC_CTL register of the Universe IID is set by code running on the DMC processor. This performs a local hard reset of the DMC board circuitry, if SW1-2 is closed, without asserting the VMEbus SYSRESET* signal.

- Another VMEbus master sets the RESET bit in the VCSR_SET register of the Universe IID over the VMEbus. In this case the LRST# signals remains asserted until the RESET bit of the VCSR_CLR register of the Universe IID is set by another VMEbus master over the VMEbus.

- The Reset Control Register in the ICH2 can be set appropriately by code running on the DMC processor.

- Let the watchdog timer time out; see Section 3.13 below.

For further information on the peripherals that play a part in the reset circuitry, refer to *Intel ® 82801BA I/O ControllerHub 2 (ICH2) and Intel ® 82801BAM I/O Controller Hub 2 Mobile (ICH2-M)* from Intel Corporation, Document Number 290687-002, and *Intel815 Chipset Family: 82815 Graphics and Memory Controller Hub (GMCH), a*lso available from Intel Corporation at www.intel.com.

3.13 Watchdog Timer Operation

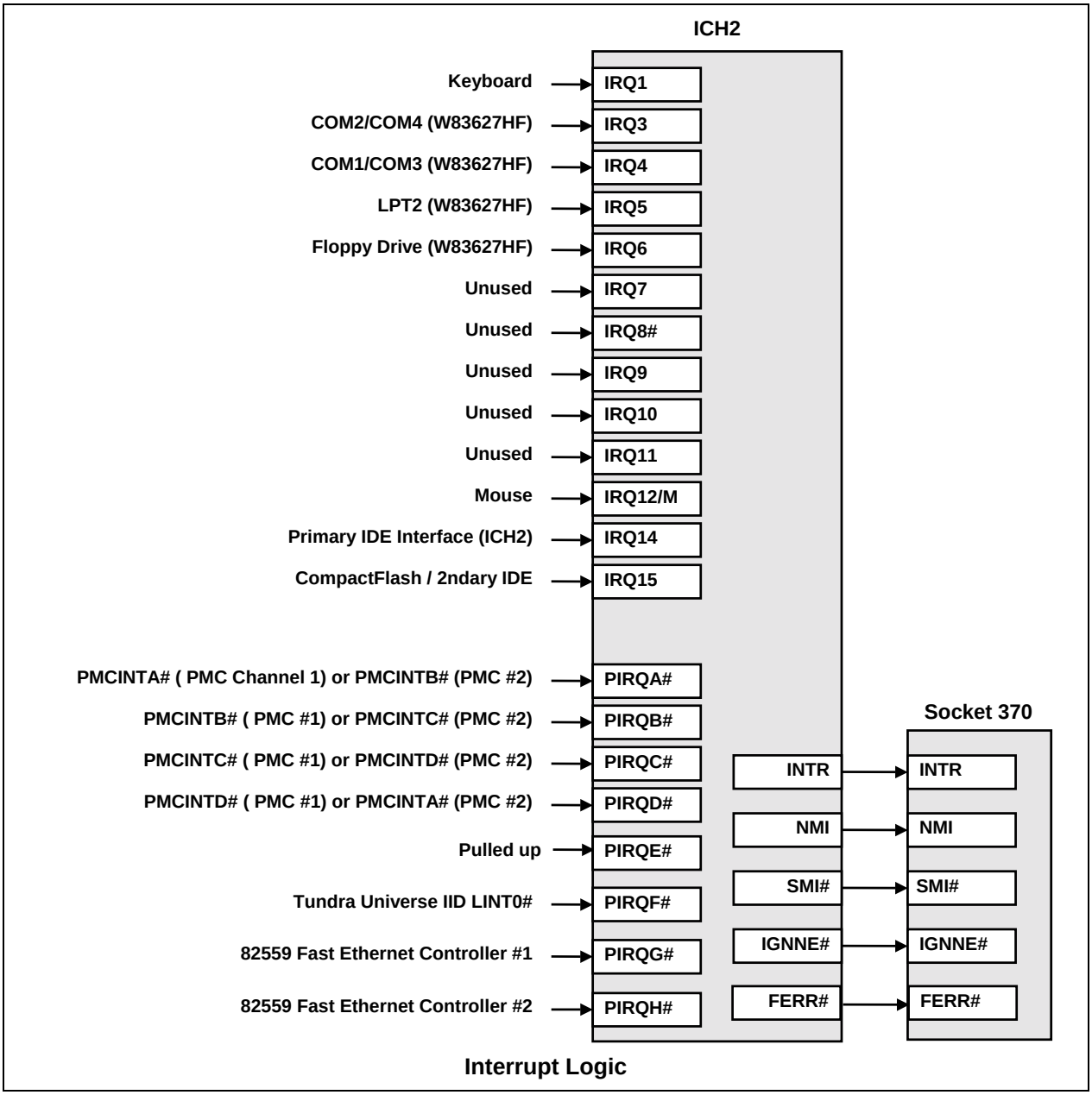
The DMC's DS1232 is used to reset the entire board through the push button accessed through the front panel, through the module's 5 VDC supply being sensed as dropping to 4.75 VDC, through a VMEbus reset if jumper SW1-2 is closed, or if the watchdog timer is enabled and it times out.

The DMC's watchdog timer is controlled by one general-purpose output line (GPO19) that is asserted by the ICH2. The DS1232 has a strobe input pin which must see an active clock. If no clock pulse is generated to the pin within 500 milliseconds, the entire DMC board will be reset. As long as GPO19 is high, a 25 MHz clock will be present at the strobe input.

To use the watchdog timer, drive GPO19 low, thereby turning off the 25 MHz clock to the DS1232's strobe input, but write a software routine that will bring GPO19 high before 500 milliseconds elapses. GPO19 is controlled by bit 19 in the ICH2's GP_LVL register. GPO19 reflects the status of bit 19: GPO19 is high if bit 19 is a logic 1 and it is low of bit 19 is at logic 0. GPO19 is high at reset so the watchdog timer will only be activated when the user drives bit 19 of the GP_LVL register low.

3.14 Interrupt Logic

The interrupt logic is shown below:



The DMC follows the standard PC ISA interrupt assignments. Logic in the ICH2 can steer the four PCI interrupts to selected ISA interrupts.

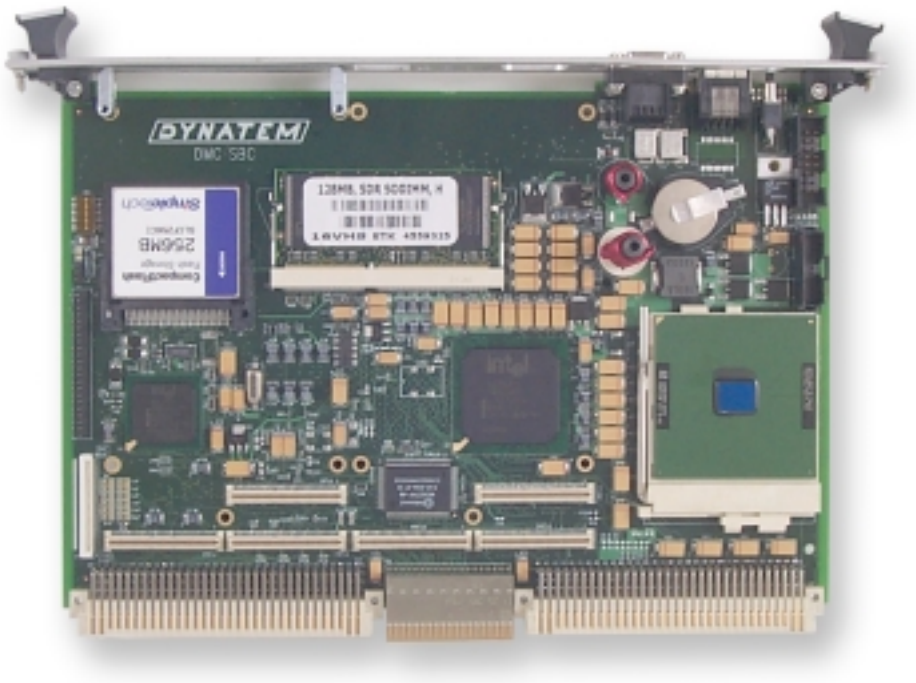
The Universe IID CA91C142D is capable of acting as an interrupter and interrupt handler for the VMEbus, and can generate PCI interrupts in response to VMEbus interrupts, VMEbus ACFAIL* being asserted, VMEbus SYSFAIL* being asserted, and various internal conditions and errors. Of the eight Universe IID LINT7# - LINT0# outputs, LINT0# is routed to the ICH2 PIRQF# input, LINT1# is pulled up with a 10K resistor, and LINT#[7:2] are pulled up via 8.2K resistors.

4. Installation

The following sections cover the steps necessary to configure the DMC and install it into a VMEbus system for single-slot operation. This chapter should be read in its entirety before proceeding with the installation.

This chapter does not discuss the installation of the DMC with the optional DxC1TB Transition Board or the connection of peripherals accessible via the DxC1TB (primary IDE, floppy drive, Ultra Wide SCSI, COM2, LPT1, and PC speaker). For information on installing the DMC with the DxC1TB Transition Board, refer to *DxC1TB Transition Board User's Manual*, available from Dynatem. Neither will I/O expansion via the rear plug-in module, the XPC2PTB, be discussed in detail.

The diagram below shows the DMC with no PMC Cards. The sections and connectors of the DMC referred to in this chapter are pointed out. The connectors that do not go to the front panel have their pin 1 location labeled. The off-board BIOS connector is for factory use.



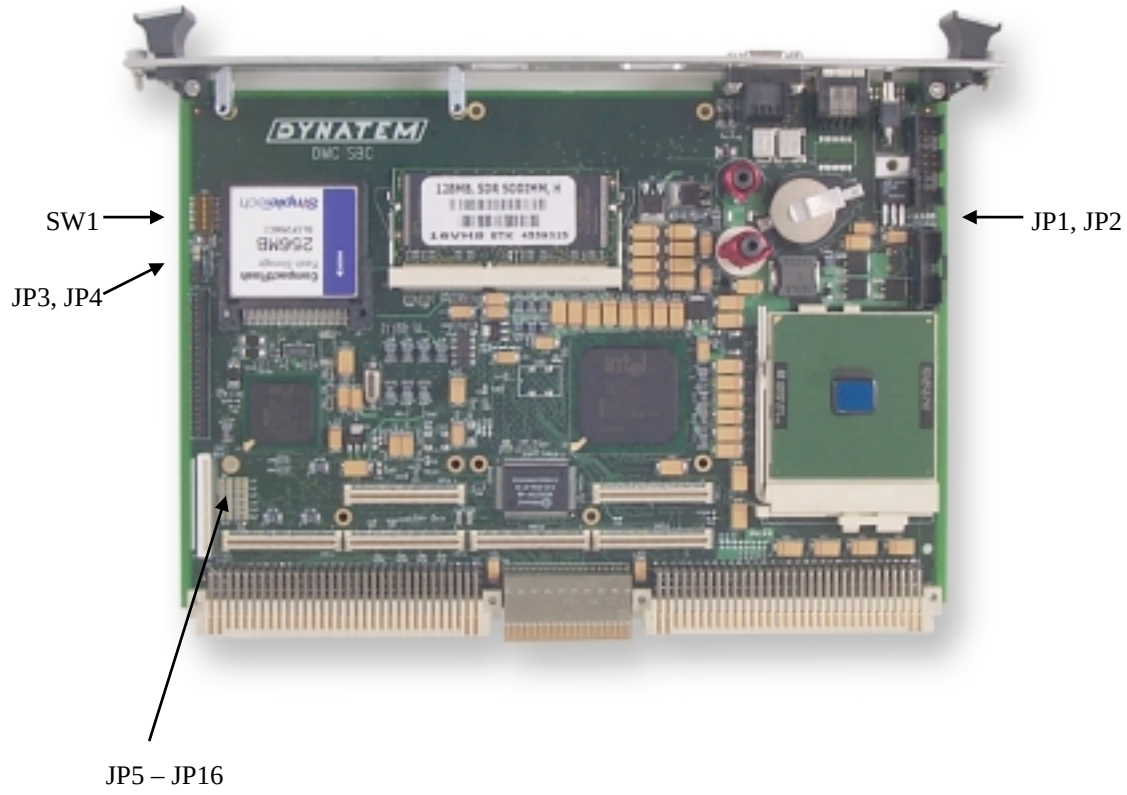
The photo above shows the DMC with a DIMM memory module and CompactFlash Drive installed.

The DMC is shipped in an antistatic bag. Be sure to observe proper handling procedures during the configuration and installation process, to avoid damage due to electrostatic discharge (ESD).

The DMC uses a heavy heat sink for cooling the Socket 370 processor. The 1.4 MHz Tualatin Pentium III CPU is a high performance device that draws a lot of current and, consequently, requires a lot of cooling.

4.1 Jumper Selectable Options

The DMC contains nine jumpers that the user should be familiar with. These jumpers are shown in the drawing below:



JP5 through JP16 will route the floppy controller's interface signals to the outer rows of the VMEbus P2 connector. This is an option that is not on the standard board. The following table summarizes all of the on-board jumpers.

The DMC offers a number of user configurable hardware options. These are set by attaching shunts to jumpers or by setting the eight position piano switch Switch 1 (SW1).

Jumpers	Description
JP1	With JP2, this jumper sets the clock rates of the SDRAM interface and CPU's Front Side Bus (FSB).
JP2	With JP1, this jumper sets the clock rates of the SDRAM I/F and CPU's FSB.
JP3	Optional 2-pin header for routing to a thermal diode for heat sensing.
JP4	For Battery Backed RTC/NVRAM. Normal: 1 & 2, to clear: 2 & 3
JP5	To route FDC line -RDATA to P2.D24 instead of PMC I/O
JP6	To route FDC line -HDSEL to P2.Z23 instead of PMC I/O
JP7	To route FDC line –TRK0 to P2.Z25 instead of PMC I/O
JP8	To route FDC line -WPT to P2.D25 instead of PMC I/O
JP9	To route FDC line -WDATA to P2.D27 instead of PMC I/O
JP10	To route FDC line -WGATE to P2.D26 instead of PMC I/O
JP11	To route FDC line -DIR to P2.D28 instead of PMC I/O
JP12	To route FDC line -STEP to P2.Z27 instead of PMC I/O
JP13	To route FDC line -DSKCHG to P2.Z29 instead of PMC I/O
JP14	To route FDC line –MOTR0 to P2D29 instead of PMC I/O
JP15	To route Floppy Disk line -INDEX to P2.Z31 instead of PMC I/O
JP16	To route FDC line -DRVS0 to P2.D30 instead of PMC I/O
Switch 1	**Description**
SW1-1	VMEbus Slot 1 Controller when open
SW1-2	DMC is reset by the VMEbus SYSRESET when closed
SW1-3	Close to permit the Universe IID to reset the VMEbus with SYSRESET
SW1-4	For Factory use. User should **keep closed**.
SW1-5	Force CPU to freq strap to safe mode when open. User should **keep open**.
SW1-6	No reboot on 2nd ICH2 Watchdog timeout when closed.
SW1-7	Close when an XPC2PTB with CODEC support is used.

Jumpers JP1 and JP2 determine both the clock speed of the DRAM interface and the clock rate of the processor's front side bus. These jumpers will be set appropriately at the factory and they should not be changed. Jumper positions and host bus and DRAM clocks are provided in the following truth table:

JP1	JP2	Front Side Bus Clock	DRAM Clock
1 - 2	1 - 2	133 MHz	100 MHz
1 - 2	2 - 3	100 MHz	100 MHz
2 - 3	1 - 2	133 MHz	133 MHz
2 - 3	2 - 3	66 MHz	100 MHz

Jumper JP3 is available for a possible thermal sensor add-on module.

Jumper JP4 is provided for clearing the NVRAM. If BIOS parameters are modified and the DMC goes into a failure mode, default variables can be restored by grounding the battery supply voltage going to the NVRAM and the RTC. This is done by momentarily shunting pins 2 & 3 of JP4 when power is off. When JP4 is shunted between pins 1 & 2, the RTC and the NVRAM draw supply voltage from the lithium coin cell on-board. As with all jumpers, pin 1 can be identified as having a square pad on the solder side of the printed circuit board.

NVRAM / RTC Battery Source	JP4
Draw Battery Voltage from On-board Coin Cell	1-2
Clear NVRAM & RTC (While Powered Down)	2-3

Battery Voltage Supply Selection

Jumpers JP5 – JP16 should be shunted if the user wishes to route the floppy disk interface to the P2 connector. Most likely this would be used with Dynatem's XPC2PTB rear plug-in module that provides a floppy disk connector for routing from behind the backplane.

When a VMEbus module occupies slot 1 of the VMEbus chassis (the slot to the extreme left), it must behave as system controller (act as multiprocessing arbiter and generate utility bus signals). Switch SW1-1 configures the VMEbus System Controller functionality of the Universe IID, as shown below:

VMEbus System Controller	SW1-1
Enabled	Open
Disabled	Closed

VMEbus System Controller Configuration

Switch SW1-2 lets VMEbus SYSRESET's reset the DMC when closed. When open, VMEbus SYSRESETs from other modules will not impact the DMC.

VMEbus SYSRESET In Selection	SW1-2
DMC Won't Receive SYSRESET's from the VMEbus	Open
DMC Receives SYSRESET's from the VMEbus	Closed

VMEbus SYSRESET In Selection

Switch SW1-3 lets DMC SYSRESETs reset the VMEbus when closed. When open, the DMC cannot drive SYSRESETs to other modules on the VMEbus. The Universe IID only drives SYSRESET when the DMC is a Slot 1 Controller.

VMEbus SYSRESET Out Selection	SW1-3
DMC Won't Drive SYSRESETs to the VMEbus	Open
DMC Drives SYSRESETs to the VMEbus	Closed

VMEbus SYSRESET Out Selection

4.2 CompactFlash Drive Installation

The DMC supports a bootable CompactFlash Drive for booting into an Operating System (OS) while occupying only one slot in the VMEbus chassis. Secondary IDE connector J6 is a Type II CompactFlash connector and is used for this purpose. J6 is located under the first PMC module, the one furthest from the Socket 370 processor. Any PMC module that may be installed in this position might obscure it. At any rate, in order to remove or install a CompactFlash drive in J6, there can be no PMC module present in PMC site #1.

4.3 PCI Mezzanine Card (PMC) Installation

The DMC supports two single-width 32-bit PCI Mezzanine Cards (PMC), each via connectors JN1 and JN2. JN4 connectors are provided for routing I/O from the PMC module to the backplane. For PMC site #1 (using connectors P1JN1, P1JN2, and P1JN4), the JN4 I/O pins are routed to the outer rows (d & z) of a 5-row VMEbus P2 connector. For PMC site #2 (using connectors P2JN1, P2JN2, and P2JN4), the JN4 I/O pins are routed to the VME64 Extensions connector P0. With either PMC site, a VME64 extensions backplane is required to route PMC I/O from JN4 to the backplane. The DMC does not use JN3 connectors because 64-bit PCI is not supported, but cards containing a PN3 connector are accommodated (i.e., no components on the DMC interfere with a PMC PN3 connector). To install a PCI Mezzanine Card, follow these steps:

1. Place the DMC on a flat surface with the VMEbus connectors towards you and the front panel away from you.

2. Insert the front panel of the PMC board through the DMC front panel opening, while keeping the PMC board at a slight angle to the DMC. This step may require some experimentation due to the EMC gasket on the PMC board that fits snugly between the PMC board front panel and the DMC front panel.

3. Line up the PN1/PN2/PN4 connectors on the PMC board with the JN1/JN2/JN4 connectors on the DMC, and gently press the PMC board into place so that the connectors mate.

4. Install the four mounting screws and washers into the PMC board mounting holes from the bottom side of the DMC.

4.4 VMEbus Chassis Installation

Unless your VMEbus chassis features automatic daisy chaining, it will have a set of five jumpers for each slot:

- **Interrupt Acknowledge** – IACKIN* and IACKOUT*
- **Bus Grant 0** – BG0IN* and BG0OUT*
- **Bus Grant 1** – BG1IN* and BG1OUT*
- **Bus Grant 2** – BG2IN* and BG2OUT*
- **Bus Grant 3** – BG3IN* and BG3OUT*

These jumpers are typically found between slots, and when configuring a VMEbus chassis, care must be taken to correctly determine the slot affected by the jumpers (the slot to the right of the jumpers). The interrupt acknowledge is a daisy chain from the board acknowledging the interrupt request to the boards that can issue an interrupt request. The bus grant signals are daisy chains from the system controller, which contains the bus arbiter, to the boards that can request the bus.

Empty VMEbus slots between boards should have all of these jumpers installed. Any slot containing the DMC should have all of these jumpers removed. Any VMEbus slots after the last board in the chassis (that is, the board

farthest away from the system controller, which is always in slot 1) do not require these jumpers. For other boards in the VMEbus chassis, refer to their installation instructions for their jumper requirements.

Once the VMEbus chassis jumpers are installed, insert the DMC into its designated slot. With the DMC ejector handles inward, firmly push the DMC into the VMEbus connectors on the chassis. Tighten the screws to the outside of the ejector handles to complete the installation of the DMC in the VMEbus chassis.

4.5 Front Panel Connections

The DMC offers front panel connections for VGA, a single connector for PS/2 style keyboard and mouse which requires a "Y" splitter cable and an adapter, an RJ45 connector for 10BaseT/100BaseTX Ethernet, and two openings for PMC front panel I/O. In order to fit the GUI connectors(mouse/kybd and VGA) in the front panel, Dynatem used ITT Cannon's MDSM connectors. These connectors require adapters, which are delivered with DMC, to support industry standard interfaces. A Y-splitter cable is also provided for routing to the mouse and keyboard. The VGA connector is to the right while the Mouse/kybd connector is to the left – when viewing the DMC while installed in a VMEbus chassis.

Install all front panel cables by inserting them into the appropriate connector. PS/2 mouse/.kybd and VGA cables can be secured to the DMC by tightening their thumbscrews into the connectors' jackscrews. Mounting hardware for the front panel connectors are isolated from the DMC's digital ground. They are continuous with the front panel itself that, in turn, is intended to be common with chassis ground.

4.6 Front Panel Reset Switch and LEDs

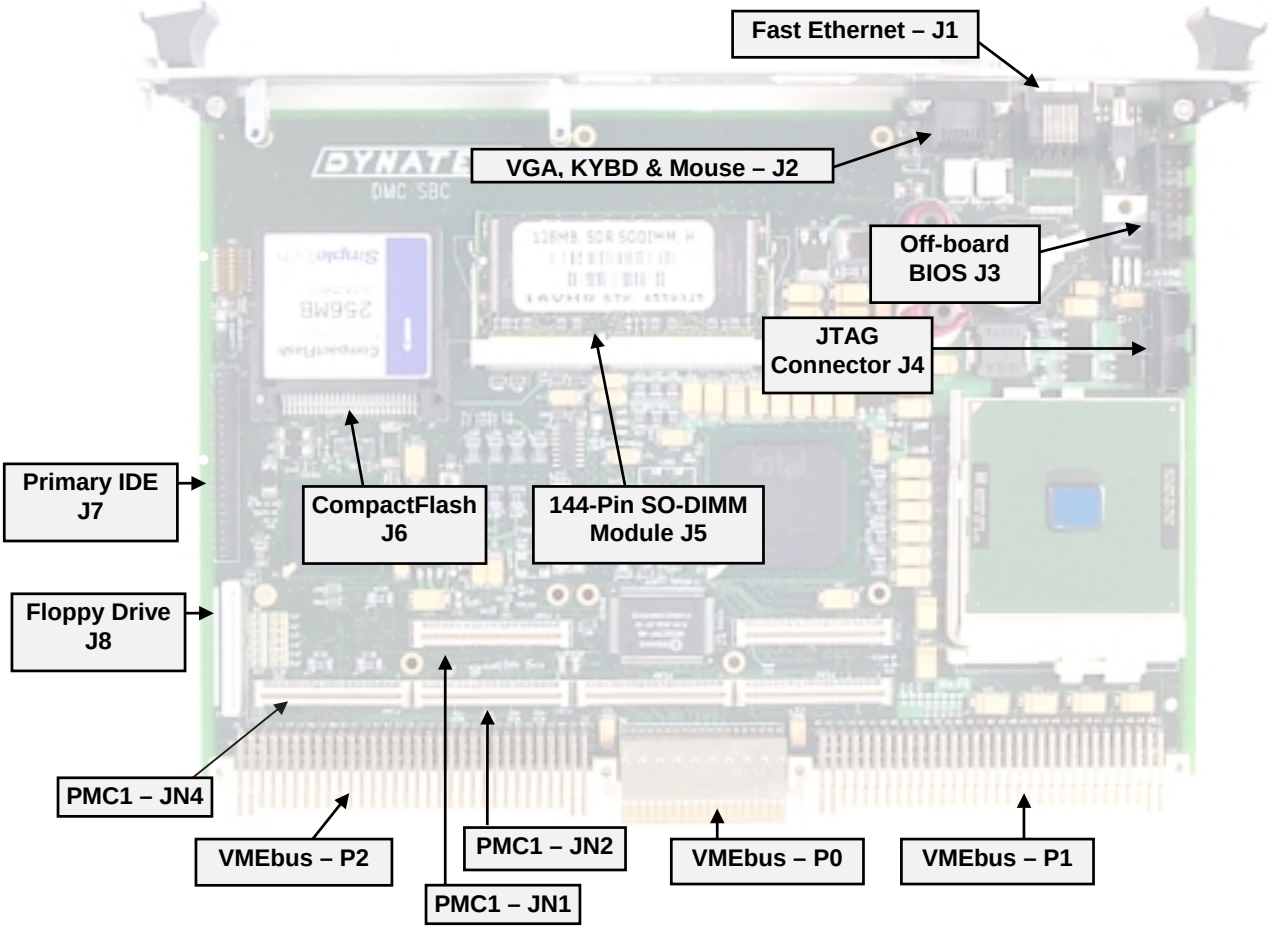
The DMC contains a recessed reset switch, accessible from the front panel. To reset the DMC, press the reset switch using a small screwdriver blade or similar object.

The DMC contains two sets of three front panel LEDs, which can be viewed through 6 tiny holes in the front panel, located around the reset button while viewing the DMC after it has been installed in the chassis. These two sets of LED's offer stats on the two 82559 Ethernet controllers on the DMC. Section 3.5 explains the locations of these two sets of LED's. Here is an explanation of their functionality:

- **Link** – Ethernet link is established when on. Labeled CR1 for the front panel Ethernet port, CR4 for the Ethernet port routed to the VMEbus backplane.
- **Activity** – Ethernet data is being transmitted or received by the DMC when on. Labeled CR2, CR5.
- **Speed** – Ethernet data is transferred at 100BaseTX rates when on. Labeled CR3, CR6.

A. Connector Pin-outs

The locations of the DMC connectors are shown below. The connectors that do not go to the front panel have their pin 1 location designated accordingly. The numbering conventions for PMC site #1 connectors are given below. PMC site #2 connectors are to the right and they follow the same convention as site #1



A.1 JTAG Debug Port (J4)

This JTAG debug connector permits in-circuit emulation for system debugging.

Pin	Signal	Pin	Signal
1	GND	2	RESET#
3	GND	4	DBRESET#
5	GND	6	TCX
7	TDI	8	TMS
9	TDO	10	POWERON
11	TRST#	12	N/C
13	N/C	14	GND
15	PREQ0#	16	GND
17	PRDY0#	18	GND
19	N/C	20	GND
21	N/C	22	GND
23	N/C	24	GND
25	N/C	26	GND
27	N/C	28	GND
29	N/C	30	ITPCLK

JTAG Connector (J4)

A.2 Floppy Drive Interface Connector (J8)

For details on the Floppy Drive Interface signals, refer to the *Winbond W83627HFManual.*

Pin	Signal Description
1	+5 VDC
2	INDEX#
3	+5 VDC
4	DS0#
5	+5 VDC
6	DSKCHG#
7	No connection
8	No connection
9	No connection
10	MTR0#
11	No connection
12	DIR#
13	No connection
14	STEP#
15	GND
16	WDATA#
17	GND
18	WGATE#
19	GND
20	TRK0#
21	GND
22	WRTPRT#
23	GND
24	RDATA#
25	GND
26	HDSEL#

Floppy Drive Interface Connector (J8) – 1.00mm ZIF Flex Circuit Connector

A.3 External BIOS Connector Pin-out (J3)

Connector J3 is a 16-pin Dual In-Line connector. J3 is used to route the DMC's firmware hub interface to an external BIOS for in-factory testing and development. This port should be of no use to the customer and the connector is not populated on the DMC. The following table shows J3's pin-out:

Pin	Signal	Pin	Signal
1	SMB Clock	2	3.3 VDC
3	SMB Data	4	PCLK_8
5	LAD0	6	LAD3
7	LAD1	8	LFRAME#
9	LAD2	10	Ground
11	PCI Reset	12	No Connect
13	No Connect	14	No Connect
15	DBRESET#	16	Ground

External BIOS (J3) – 16-pin Dual-row 0.1" Header

A.4 10BaseT/100BaseTX Fast Ethernet Connector (J1)

Pin	Signal Description
1	Transmit Data + (TX+)
2	Transmit Data - (TX-)
3	Receive Data + (RX+)
4	Transmit Center Tap 1 (CTTX1)
5	Transmit Center Tap 2 (CTTX2)
6	Receive Data - (RX-)
7	Receive Center Tap 1 (CTRX1)
8	Receive Center Tap 2 (CTRX2)

10BaseT/100BaseTX Fast Ethernet Connector (J1) – Front Panel RJ-45 Connector. The metal shell of the connector goes to chassis ground.

A.5 VGA Connector (J2-1)

Pin	Signal Description
1	Red Output
2	Green Output
3	Blue Output
4	No connection
5	HSYNC/VSYNC Return (GND)
6	Red Return (GND)
7	Green Return (GND)
8	Blue Return (GND)
9	+5 VDC
10	HSYNC/VSYNC Return (GND)
11	No connection
12	DDCDAT
13	Horizontal Sync (HSYNC) Output
14	Vertical Sync (VSYNC) Output
15	DDCCLK

VGA Connector (J2-1) – Front Panel MDSM Connector. The metal shell of the connector goes to chassis ground.

Connector J2-1 is the upper half of a stacked ITT Cannon MDSM-30 connector. It will be the half that is furthest to the right when viewing the DMC while it is inserted into a VMEbus chassis. The PS/2 mouse/keyboard connector will be the other, lower, part to its left. While the pinout is the same as with an industry standard VGA connector, mechanically it is too small and incompatible so Dynatem provides an adapter cable for the MDSM termination that will mate with a VGA monitor's cable.

A.6 PS/2 Keyboard/Mouse Connector (J2-2)

Pin	Signal Description
B11	Keyboard Data
B3	Mouse Data
B10, B12	GND
B2, B4	+5 VDC (via 1 amp self-resetting fuse F1)
B9	Keyboard Clock
B1	Mouse Clock

Keyboard/Mouse Connector (J2-2) – Front Panel Mini-DIN Receptacle. The metal shell of the connector goes to chassis ground.

Connector J2-2 is the lower half of a stacked ITT Cannon MDSM-30 connector. It will be the half that is closer to the DMC's Printed Circuit Board (PCB). The VGA connector will be the other, upper, part. Dynatem provides a Y-splitter adapter cable for the MDSM termination that connects with PS/2 mouse and keyboard devices.

A.7 Primary IDE Interface Connector (J7)

Pin	Signal	Pin	Signal
1	RST#	2	GND
3	D7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	GND	20	No connection
21	DMARQ0	22	GND
23	IOW#	24	GND
25	IOR#	26	GND
27	IORDY	28	470-ohm pull-down
29	DMAACK0	30	GND
31	IRQ14	32	No connection
33	DA1	34	P66 Detect
35	DA0	36	DA2
37	CS1Fx	38	CS3Fx
39	LED Control	40	GND
41	+5 VDC	42	+5 VDC
43	GND	44	No connection

Primary IDE Interface Connector (J7) – 44-pin Dual-row 2-mm Header

A.8 CompactFlash Interface Connector (J6)

Pin	Signal	Pin	Signal
1	GND	26	CMPFLASHDET
2	D3	27	D11
3	D4	28	D12
4	D5	29	D13
5	D6	30	D14
6	D7	31	D15
7	CS1#	32	CS3#
8	GND	33	No connection
9	GND	34	DIOR#
10	GND	35	DIOW#
11	GND	36	+5 VDC
12	GND	37	DIRQ (IRQ15)
13	+5 VDC	38	+5 VDC
14	GND	39	GND (master)
15	GND	40	No connection
16	GND	41	IDERESET
17	GND	42	DIORDY
18	DA2	43	No connection
19	DA1	44	+5 VDC
20	DA0	45	No connection
21	D0	46	Pull-up to +5 VDC
22	D1	47	D8
23	D2	48	D9
24	No connection	49	D10
25	No connection	50	GND

CompactFlash Type II Interface Connector (J6)

A.9 PCI Mezzanine Card (PMC) Connectors (JN1 and JN2)

This section has the pin-outs for both PMC sites. PMC site #1 is further away from the socket 370 processor and closer to the lower edge of the module while PMC site #2 is located in the middle of the module. The JN4 pin-outs will not be given here as the signals on these connectors are routed to VMEbus connectors P2 and P0, for PMC sites 1 and 2 respectively. Please refer to section A.10 for these pin-outs.

Pin	Signal	Pin	Signal
1	5.6K pull-down	2	-12 VDC
3	GND	4	PIRQ#A
5	PIRQ#B	6	PIRQ#C
7	No connection	8	+5 VDC
9	PIRQ#D	10	No connection
11	GND	12	No connection
13	PCI CLK	14	GND
15	GND	16	PCI GNT0#
17	PCI REQ0#	18	+5 VDC
19	+5 VDC (VI/O)	20	AD31
21	AD28	22	AD27
23	AD25	24	GND
25	GND	26	C/BE3#
27	AD22	28	AD21
29	AD19	30	+5 VDC
31	+5 VDC (VI/O)	32	AD17
33	FRAME#	34	GND
35	GND	36	IRDY#
37	DEVSEL#	38	+5 VDC
39	GND	40	LOCK#
41	SDONE	42	SBO
43	PAR	44	GND
45	+5 VDC (VI/O)	46	AD15
47	AD12	48	AD11
49	AD9	50	+5 VDC
51	GND	52	C/BE0#
53	AD6	54	AD5
55	AD4	56	GND
57	+5 VDC (VI/O)	58	AD3
59	AD2	60	AD1
61	AD0	62	+5 VDC
63	GND	64	REQ64 (2.7K pull-up)

PCI Mezzanine Card (PMC) Site #1 Connector (P1JN1) – Molex 52763-0649

Pin	Signal	Pin	Signal
1	+12 VDC	2	TRST (pulled down)
3	TMS (pulled up)	4	No connection
5	TDI (pulled up)	6	GND
7	GND	8	No connection
9	No connection	10	No connection
11	+5 VDC	12	+3.3 VDC
13	PCI RST#	14	GND
15	+3.3 VDC	16	GND
17	No connection	18	GND
19	AD30	20	AD29
21	GND	22	AD26
23	AD24	24	+3.3 VDC
25	AD16 (IDSEL)	26	AD23
27	+3.3 VDC	28	AD20
29	AD18	30	GND
31	AD16	32	C/BE2#
33	GND	34	No connection
35	TRDY#	36	+3.3 VDC
37	GND	38	STOP#
39	PERR#	40	GND
41	+3.3 VDC	42	SERR#
43	C/BE1#	44	GND
45	AD14	46	AD13
47	GND	48	AD10
49	AD8	50	+3.3 VDC
51	AD7	52	No connection
53	+3.3 VDC	54	No connection
55	No connection	56	GND
57	No connection	58	No connection
59	GND	60	No connection
61	ACK64 (2.7K pull-up)	62	+3.3 VDC
63	GND	64	No connection

PCI Mezzanine Card (PMC) Site #1 Connector (P1JN2) – Molex 52763-0649

Note: PMC Connector P1JN4 is strictly for I/O routing so there is no defined pin-out assignment. Section A.10, on the following pages, shows how the P1JN4 lines are routed to the outer rows of VME64 Extensions connector P2 (some of these lines are shared with an optional FDC routing to P2).

Pin	Signal	Pin	Signal
1	5.6K pull-down	2	-12 VDC
3	GND	4	PIRQ#B
5	PIRQ#C	6	PIRQ#D
7	No connection	8	+5 VDC
9	PIRQ#A	10	No connection
11	GND	12	No connection
13	PCI CLK	14	GND
15	GND	16	PCI GNT1#
17	PCI REQ1#	18	+5 VDC
19	+5 VDC (VI/O)	20	AD31
21	AD28	22	AD27
23	AD25	24	GND
25	GND	26	C/BE3#
27	AD22	28	AD21
29	AD19	30	+5 VDC
31	+5 VDC (VI/O)	32	AD17
33	FRAME#	34	GND
35	GND	36	IRDY#
37	DEVSEL#	38	+5 VDC
39	GND	40	LOCK#
41	SDONE	42	SBO
43	PAR	44	GND
45	+5 VDC (VI/O)	46	AD15
47	AD12	48	AD11
49	AD9	50	+5 VDC
51	GND	52	C/BE0#
53	AD6	54	AD5
55	AD4	56	GND
57	+5 VDC (VI/O)	58	AD3
59	AD2	60	AD1
61	AD0	62	+5 VDC
63	GND	64	REQ64 (2.7K pull-up)

PCI Mezzanine Card (PMC) Site #2 Connector (P2JN1) – Molex 52763-0649

Pin	Signal	Pin	Signal
1	+12 VDC	2	TRST (pulled down)
3	TMS (pulled up)	4	No connection
5	TDI (pulled up)	6	GND
7	GND	8	No connection
9	No connection	10	No connection
11	+5 VDC	12	+3.3 VDC
13	PCI RST#	14	GND
15	+3.3 VDC	16	GND
17	No connection	18	GND
19	AD30	20	AD29
21	GND	22	AD26
23	AD24	24	+3.3 VDC
25	AD17 (IDSEL)	26	AD23
27	+3.3 VDC	28	AD20
29	AD18	30	GND
31	AD16	32	C/BE2#
33	GND	34	No connection
35	TRDY#	36	+3.3 VDC
37	GND	38	STOP#
39	PERR#	40	GND
41	+3.3 VDC	42	SERR#
43	C/BE1#	44	GND
45	AD14	46	AD13
47	GND	48	AD10
49	AD8	50	+3.3 VDC
51	AD7	52	No connection
53	+3.3 VDC	54	No connection
55	No connection	56	GND
57	No connection	58	No connection
59	GND	60	No connection
61	ACK64 (2.7K pull-up)	62	+3.3 VDC
63	GND	64	No connection

PCI Mezzanine Card (PMC) Site #2 Connector (P2JN2) – Molex 52763-0649

Note: PMC Connector P2JN4 is strictly for I/O routing so there is no defined pin-out assignment. Section A.10, on the following pages, shows how the P2JN4 lines are routed to the VME64 Extensions connector P0.

A.10 VMEbus Connectors (P0, P1, and P2)

Pin	Signal	Pin	Signal	Pin	Signal
A01	D00	B01	BBSY*	C01	D08
A02	D01	B02	BCLR*	C02	D09
A03	D02	B03	ACFAIL*	C03	D10
A04	D03	B04	BG0IN*	C04	D11
A05	D04	B05	BG0OUT*	C05	D12
A06	D05	B06	BG1IN*	C06	D13
A07	D06	B07	BG1OUT*	C07	D14
A08	D07	B08	BG2IN*	C08	D15
A09	GND	B09	BG2OUT*	C09	GND
A10	SYSCLK	B10	BG3IN*	C10	SYSFAIL*
A11	GND	B11	BG3OUT*	C11	BERR*
A12	DS1*	B12	BR0*	C12	SYSRESET*
A13	DS0*	B13	BR1*	C13	LWORD*
A14	WRITE*	B14	BR2*	C14	AM5
A15	GND	B15	BR3*	C15	A23
A16	DTACK*	B16	AM0	C16	A22
A17	GND	B17	AM1	C17	A21
A18	AS*	B18	AM2	C18	A20
A19	GND	B19	AM3	C19	A19
A20	IACK*	B20	GND	C20	A18
A21	IACKIN*	B21	No connection (NC)	C21	A17
A22	IACKOUT*	B22	No connection (NC)	C22	A16
A23	AM4	B23	GND	C23	A15
A24	A07	B24	IRQ7*	C24	A14
A25	A06	B25	IRQ6*	C25	A13
A26	A05	B26	IRQ5*	C26	A12
A27	A04	B27	IRQ4*	C27	A11
A28	A03	B28	IRQ3*	C28	A10
A29	A02	B29	IRQ2*	C29	A09
A30	A01	B30	IRQ1*	C30	A08
A31	-12 VDC	B31	+5 VDC Standby (NC)	C31	+12 VDC
A32	+5 VDC	B32	+5 VDC	C32	+5 VDC

VMEbus Connector (P1) – DIN 41612 96-pin (3 rows x 32 pins)

The JN4 lines from PMC site #1 are routed to the P2 connector but the Floppy Disk Controller (FDC) signals may also be routed to rows D & Z of P2 by shunting jumpers JP5 through JP16. ***Be careful that these lines don't overlap.*** The XMCPTB rear plug-in expansion module supports P2 FDC expansion with an FDC connector. The optional FDC signals (only routed to the backplane when JP5 through JP16 are closed) are in bold and the corresponding P1JN4 pin numbers are in parentheses (always routed to the backplane).

One difference between the P2 routing of the DMC and previous Dynatem cards, that expanded through the adjacent slot transition module (the TB) or the rear plug-in card (XPC2PTB), is that the DMC routes the second Ethernet port out through P2. So pins A16 and A17 used to be tied together on the XPC2PTB for SCSI power, pin C12 used to be used for ground, and C13 used to be used for an optional battery voltage. Now all four of these pins are used for the 2nd Ethernet port. ***Care must be taken to use an XMCPTB or the TBM with the DMC***. Please call Dynatem for support if you wish to use earlier versions of these transition modules (for the DRC1 and the DPC2) with the DMC.

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
Z01	P1JN4-pin2	A01	IDE PDREQ	B01	+5 VDC	C01	COM1 TxD	D01	P1JN4-pin1
Z02	GND	A02	IDE PDIOW#	B02	GND	C02	COM1 RxD	D02	P1JN4-3
Z03	P1JN4-5	A03	IDE PDIOR#	B03	No Connect	C03	COM1 RTS	D03	P1JN4-4
Z04	GND	A04	IDE PDIORDY	B04	A24	C04	COM1 CTS	D04	P1JN4-6
Z05	P1JN4-8	A05	IDE PDDACK#	B05	A25	C05	COM1 DTR	D05	P1JN4-7
Z06	GND	A06	IDE PDIRQ	B06	A26	C06	COM1 DSR	D06	P1JN4-9
Z07	P1JN4-11	A07	IDE PDA1	B07	A27	C07	COM1 DCD	D07	P1JN4-10
Z08	GND	A08	IDE PDA0	B08	A28	C08	COM1 RI	D08	P1JN4-12
Z09	P1JN4-14	A09	IDE PDCS1#	B09	A29	C09	P1JN4-28	D09	P1JN4-13
Z10	GND	A10	IDE RSTDRV#	B10	A30	C10	Speaker Output	D10	P1JN4-15
Z11	P1JN4-17	A11	IDE PDA2	B11	A31	C11	+5 VDC	D11	P1JN4-16
Z12	GND	A12	IDE PDCS3#	B12	GND	C12	LAN2RDP	D12	P1JN4-18
Z13	P1JN4-20	A13	IDE PDD7	B13	+5 VDC	C13	LAN2RDN	D13	P1JN4-19
Z14	GND	A14	IDE PDD6	B14	D16	C14	IDE LED#	D14	P1JN4-21
Z15	P1JN4-23	A15	GND	B15	D17	C15	P1JN4-30	D15	P1JN4-22
Z16	GND	A16	LAN2TDP	B16	D18	C16	LPT1 STROBE#	D16	P1JN4-24
Z17	P1JN4-26	A17	LAN2TDN	B17	D19	C17	LPT1 AUTOFD#	C17	P1JN4-25
Z18	GND	A18	IDE PDD15***	B18	D20	C18	LPT1 PD0	D18	P1JN4-27
Z19	P1JN4-29	A19	IDE PDD5	B19	D21	C19	LPT1 ERR#	D19	P1JN4-28
Z20	GND	A20	GND	B20	D22	C20	LPT1 PD1	D20	P1JN4-30
Z21	P1JN4-32	A21	IDE PDD4	B21	D23	C21	LPT1 INIT#	D21	P1JN4-31
Z22	GND	A22	IDE PDD3	B22	GND	C22	LPT1 PD2	D22	P1JN4-33
Z23	**Hdsel#** (35)	A23	IDE PDD2	B23	D24	C23	LPT1 SLCTIN#	D23	P1JN4-34
Z24	GND	A24	IDE PDD1	B24	D25	C24	LPT1 PD3	D24	**Rdata#** (36)
Z25	**Trk0#** (38)	A25	IDE PDD0	B25	D26	C25	LPT1 PD4	D25	**Wpt#** (37)
Z26	GND	A26	IDE PDD8	B26	D27	C26	LPT1 PD5	D26	**Wgate#** (39)
Z27	**Step#** (41)	A27	IDE PDD9	B27	D28	C27	LPT1 PD6	D27	**Wdata#** (40)
Z28	GND	A28	IDE PDD10	B28	D29	C28	LPT1 PD7	D28	**Dir#** (42)
Z29	**Dskchg#** (44)	A29	IDE PDD11	B29	D30	C29	LPT1 ACK#	D29	**Motr0#** (43)
Z30	GND	A30	IDE PDD12	B30	D31	C30	LPT1 BUSY	D30	**Drvs0#** (45)
Z31	**Index#** (46)	A31	IDE PDD13	B31	GND	C31	LPT1 PE	D31	GND
Z32	GND	A32	IDE PDD14	B32	+5 VDC	C32	LPT1 SLCT	D32	+5 VDC

VMEbus Connector (P2) – 160-pin (5 rows x 32 pins)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A01	P2JN4-56	B01	P2JN4-57	C01	P2JN4-58	D01	P2JN4-59	E01	P2JN4-60
A02	P2JN4-51	B02	P2JN4-52	C02	P2JN4-53	D02	P2JN4-54	E02	P2JN4-55
A03	P2JN4-46	B03	P2JN4-47	C03	P2JN4-48	D03	P2JN4-49	E03	P2JN4-50
A04	P2JN4-41	B04	P2JN4-42	C04	P2JN4-43	D04	P2JN4-44	E04	P2JN4-45
A05	P2JN4-36	B05	P2JN4-37	C05	P2JN4-38	D05	P2JN4-39	E05	P2JN4-40
A06	P2JN4-31	B06	P2JN4-32	C06	P2JN4-33	D06	P2JN4-34	E06	P2JN4-35
A07	P2JN4-26	B07	P2JN4-27	C07	P2JN4-28	D07	P2JN4-29	E07	P2JN4-30
A08	P2JN4-21	B08	P2JN4-22	C08	P2JN4-23	D08	P2JN4-24	E08	P2JN4-25
A09	P2JN4-16	B09	P2JN4-17	C09	P2JN4-18	D09	P2JN4-19	E09	P2JN4-20
A10	P2JN4-11	B10	P2JN4-12	C10	P2JN4-13	D10	P2JN4-14	E10	P2JN4-15
A11	P2JN4-6	B11	P2JN4-7	C11	P2JN4-8	D11	P2JN4-9	E11	P2JN4-10
A12	P2JN4-1	B12	P2JN4-2	C12	P2JN4-3	D12	P2JN4-4	E12	P2JN4-5
A13	COM2 CTS	B13	COM2 DTR	C13	COM2 RI	D13	COM2 RTS	E13	No Connect
A14	COM2 DCD	B14	COM2 DSR	C14	COM2 RxD	D14	USB #1 N	E14	COM2 TxD
A15	USB Over A	B15	USB #0 N	C15	USB #0 P	D15	Mouse Data	E15	USB #1 P
A16	MIDI In	B16	Kybd Data	C16	Kybd Clock	D16	Joy2 Button2	E16	Mouse Clock
A17	MIDI Out	B17	Joy2 Y	C17	Joy1 Y	D17	Joy1 X	E17	Joy1 Button2
A18	AC '97 Clock	B18	Joy1 Button1	C18	Joy2 Button1	D18	AC '97 Data In	E18	Joy2 X
A19	InfraRed RxD	B19	InfraRed TxD	C19	AC '97 Reset	D19	AC '97 Data Out	E19	AC '97 SYNC

VME64 Extensions Bus Connector (P0)

B. Address Maps, Interrupts, DMA Channels

Tables of the DMC's address maps, interrupt request assignments, and DMA channel usage are given in the following sections. All addresses are shown in hexadecimal notation.

B.1 Memory Map

The DMC's memory map is shown below:

Address Range	Description
00000000 - 0009FFFF	DOS area main memory (640 KB)
000A0000 – 000BFFFF	Std PCI/ISA Video Memory (128 KB)
000C0000 – 000FFFFF	BIOS Region
00100000 – 1FFFFFFF	DRAM (up to 512 MB)
01000000 – FFFFFFFF:	PCI Memory Address Range breaks as:
FEC00000 - FECFFFFF, FEE00000 - FEEFFFFF	APIC Configuration Area (unused on DMC)
FFFC0000 - FFFFFFFF	High BIOS Area

For further details on the DMC memory space map, refer to Section 4.1.1 in *Intel 815E Chipset Family:82815 Graphics and Memory Controller Hub (GMCH)* data sheet, available from Intel Corporation.

B.2 PCI Configuration Space Map

The PCI configuration space map is shown below. The Vendor ID and Device ID in hex for the PMC slot are shown as *xxxx*, since they depend on the type of device installed in the PMC slot.

IDSEL	Bus	Dev	Fcn	VenID	DevID	Description
—	00	00	0	8086	1130	GMCH Host Bridge/Controller
—	00	30	0	8086	244E	82801BA PCI-ISA Bridge
—	00	31	0	8086	2440	82801BA Low Pin Count (LPC) Interface
—	00	31	0	8086	2440	82801BA DMA Operation
—	00	31	0	8086	2440	82801BA Timers
—	00	31	0	8086	2440	82801BA Interrupt Controllers (PIC)
—	00	31	0	8086	2440	82801BA Advanced Interrupt Controllers (APIC)
—	00	31	0	8086	2440	82801BA Real Time Clock (PIC)
—	00	31	0	8086	2440	82801BA Power Mgmt & DMC Watchdog
—	00	31	1	8086	244b	82801BA PCI-IDE Interface
—	00	31	2,4	8086	2442	82801BA PCI-USB Interface
AD23	001	7	0	8086	1229	82559 Fast Ethernet Controller #1
AD24	001	8	0	8086	1229	82559 Fast Ethernet Controller #2
AD16	001	0	0	xxxx	xxxx	PCI Mezzanine Card (PMC) Slot #1
AD17	001	1	0	xxxx	xxxx	PCI Mezzanine Card (PMC) Slot #2
AD27	001	11	0	10E3	0000	Universe IID CA91C142D PCI-VMEbus Interface

For further details refer to *Intel 82801BA I/O Controller Hub 2(ICH2) and Intel 82801BAM I/O Controller Hub 2 Mobile (ICH2-M)* data sheet, available from Intel Corporation.

B.3 Interrupt Request Routing

The ISA interrupt request routing is shown below:

IRQ	Description
0	Timer 0 (ICH2)
1	Keyboard (W83627HF's keyboard/mouse controller)
2	Cascade Interrupt from slave PIC (ICH2)
3	COM2/COM4 (W83627HF)
4	COM1/COM3 (W83627HF)
5	Assigned to a PCI IRQ by the BIOS
6	Floppy Drive (W83627HF)
*7	LPT1 (W83627HF)
8	Real Time Clock (ICH2)
9	Assigned to a PCI IRQ by the BIOS
10	Assigned to a PCI IRQ by the BIOS
11	Assigned to a PCI IRQ by the BIOS
12	Mouse (W83627HF's keyboard/mouse controller)
13	Math Coprocessor (ICH2)
14	Primary IDE Interface (ICH2)
15	Secondary IDE Interface (ICH2, via MIRQ0)

The PCI interrupt request routing to the Intel 82801BA PCI-ISA Bridge (ICH2) is shown below:

ICH2 PCI IRQ	Description
See Section A.9	PMC Site #1 INTA#, INTB#, INTC#, INTD#
See Section A.9	PMC Site #2 INTB#, INTC#, INTD#, INTA#
PIRQH#	Intel 82559 #1
PIRQG#	Intel 82559 #2
PIRQF#	Tundra Universe IID CA91C142D LINT0#

For further details on interrupts, refer to the documentation for the various peripherals that generate interrupts, as well as *Intel 82801BA I/O Controller Hub 2(ICH2) and Intel 82801BAM I/O Controller Hub 2 Mobile (ICH2-M)* data sheet, available from Intel Corporation. Note: the DMC uses the ICH2 and not the ICH2-M.

B.4 ISA DMA Channel Assignments

The ISA DMA channel assignments are shown below:

DMA Channel	Description
0	Super I/O chip DMA Channel 0
1	DMA Channel 1
2	DMA Channel 2
3	DMA Channel 3
4	No connection
5	No connection
6	No connection
7	No connection

5.6K resistors pull down all DMA Request lines. For further details on ISA DMA channel usage, refer to *Intel 82801BA I/O Controller Hub 2(ICH2) and Intel 82801BAM I/O Controller Hub 2 Mobile (ICH2-M)* data sheet, available from Intel Corporation, as well as the *W83627HF Data Sheet*, available from Winbond.

B.5 PCI Bus Request/Grant Routing

The PCI bus request/grant routing to the ICH2 is shown below:

TXC REQ#/GNT#	Description
REQ0#/GNT0#	PMC Site #1 REQ#/GNT#
REQ1#/GNT1#	PMC Site #2 REQ#/GNT#
REQ2#/GNT2#	Intel 82559 #1 REQ#/GNT#
REQ3#/GNT3#	Intel 82559 #1 REQ#/GNT#
REQ4#/GNT4#	Tundra Universe IID CA91C142D REQ#/GNT#

For further details on the PCI bus request/grant signals, refer to *Intel 815E Chipset Family:82815 Graphics and Memory Controller Hub (GMCH)* data sheet, available from Intel Corporation.

C. Power and Environmental Requirements

The DMC power and environmental requirements are shown in the tables below.

Condition	Power Requirements
1.26 GHz Pentium III, 512 KB on-die L2 Cache	+5 VDC @ 5.9 A typ. +12 VDC @ 0.21 mA typ.

Power Requirements

Condition	Environmental Requirements
Operating Temperature	0° to +70° C
Storage Temperature	-50° to +105° C

Environmental Requirements