DPM/RPM VMEbus Pentium M Based Single Board Computer

User's Manual

xPM User’s Manual Rev. 2.02

December 2008

Dynatem

23263 Madero, Suite C

Mission Viejo, CA 92691

Phone: (949) 855-3235

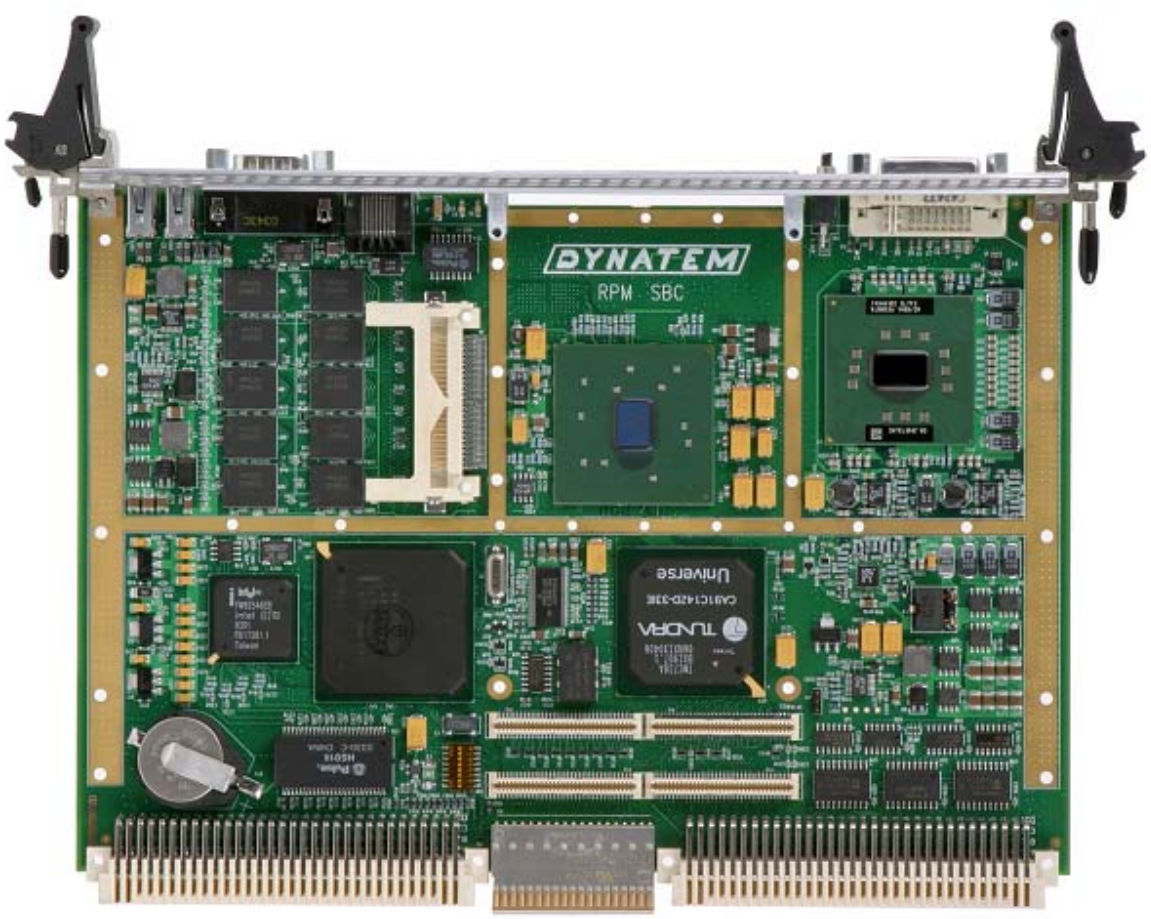
Fax: (949) 770-3481

www.dynatem.com

Table of Contents

1. Features

The Dynatem xPM is a single-slot 6U VMEbus Single Board Computer (SBC). The xPM offers full PC performance with a Pentium M low-power processor. The xPM is available in two versions: the lower cost DPM for standard industrial applications and the 1101.2 compliant, conduction-cooled RPM with wedgelocks, stiffener bar, and a full board heatsink for rugged applications. When referring to attributes of both versions, we will use the common name xPM. The xPM employs Intel's embedded technology to assure long-term availability.



Features of the xPM include:

- Single-slot VMEbus operation with on-board CompactFlash disk for bootable mass storage and front panel connectors for two USB 2.0 ports, DVI-I Graphics, a 10/100BaseTX port, PMC I/O, and a COM1 port.

- IDE and the Low Pin Count (LPC) interface are routed out to the backplane via the P2 connector, the LPC interface routes to a Super I/O device for COM3/4, Floppy Interface, LPT1, and mouse/keyboard on the rear plug-in card – or two more USB 2.0 ports and two COM ports are routed to P2 instead of the LPC.

- PMC I/O, two Serial ATA ports, AC '97 Codec interface, two Gbit Ethernet ports (Vita 31.1 compliant) and the DVI-I Graphics port are routed to P0.

- The Intel® 855GME Graphics Memory Controller Hub (GMCH) and Intel® 6300ESB I/O Controller Hub (ICH) provide high-speed memory control, built-in graphics, integrated I/O like Serial ATA, USB 2.0, IDE supporting Ultra 100 DMA Mode for transfers up to 88.88 MB/sec, and 64 bit PCI-X bus transfers at 66 MHz.
- Intel's 82559 10/100BaseTX interface accessible at the front panel.
- Intel's 82546 Ethernet Controller offers two 10/100/1000BaseTX support routed to P0 in compliance with Vita 31.1 for backplane fabric switching.
- Up to 1 GB of DDR DRAM provided on-board.
- Tundra Universe IID PCI-VMEbus Interface provides 64-bit VMEbus transfer rates over 30 MB/sec. Integral FIFOs permit write-posting to maximize available PCI and VMEbus bandwidth. Full Slot 1 (System Controller) functionality is provided.
- PCI Mezzanine Card (PMC) expansion is supported 64 bits @ up to 66 MHz.
- Secondary IDE port for CompactFlash on-board for flash-based or mechanical mass storage for 1 slot booting
- General Software's flash-based system BIOS.
- PXE for diskless booting over Ethernet.
- Programmable watchdog timer for system recovery.
- Operating System (OS) and driver support, including Windows NT, Embedded NT, XP, QNX, VxWorks, Linux, Solaris, and pSOS+.

2. Related Documents

Listed below are documents that describe the Pentium processor and chipset, and the peripheral components used on the xPM. Either download from the Internet or contact your local distributor for copies of these documents.

The xPM uses the Low Voltage Pentium M. For information on this processor, go to:

http://www.intel.com/design/intarch/pentiumm/pentiumm.htm

For the ICH component in the 6300ESBchipset get the *Intel ® 6300ESB I/O Controller Hub Datasheet*. It is document number 300641-002.

ftp://download.intel.com/design/intarch/datashts/30064102.pdf

For the GMCH component in the chipset get the *Intel ® 855GM/855GME Chipset Graphics and Memory Controller Hub (GMCH) Datasheet*. It is document number 252615-004.

ftp://download.intel.com/design/chipsets/datashts/25261504.pdf

For data sheets on I/O controllers:

- *82546EB Fast Ethernet PCI Controller*
  http://developer.intel.com/design/network/products/lan/controllers/82546.htm

- *82559 Ethernet PCI Controller*
  http://www.intel.com/design/network/products/lan/controllers/82559.htm

- *VMEbus Interface Components Manual*
  Tundra Semiconductor Corporation; Universe IID revisions are found at www.tundra.com

The following documents provide information on the PC architecture and I/O:

- *PCI Local Bus Specification, Revision 2.2*
  http://www.pcisig.com/specifications/

- *PCI-X Specification, Revision 1.0A*
  http://www.pcisig.com/specifications/

- *System Management Bus Specification (SMBus), Revision 1.1*
  http://www.smbus.org/specs/

- *Universal Serial Bus Specification*
  http://www.usb.org/developers

The following documents cover topics relevant to the VMEbus and can be purchased through VITA:

- IEEE Std 1014-1987, *IEEE Standard for a Versatile Backplane Bus: VMEbus*
  The Institute of Electrical and Electronic Engineers
  345 East 47th Street
  New York, NY 10017
  (800) 678-4333

- Wade D. Peterson, *The VMEbus Handbook*
  VITA
  10229 North Scottsdale Road, Suite B
  Scottsdale, AZ 85253
  (480) 951-8866

The following documents are the current draft standards for the PCI Mezzanine Card (PMC):

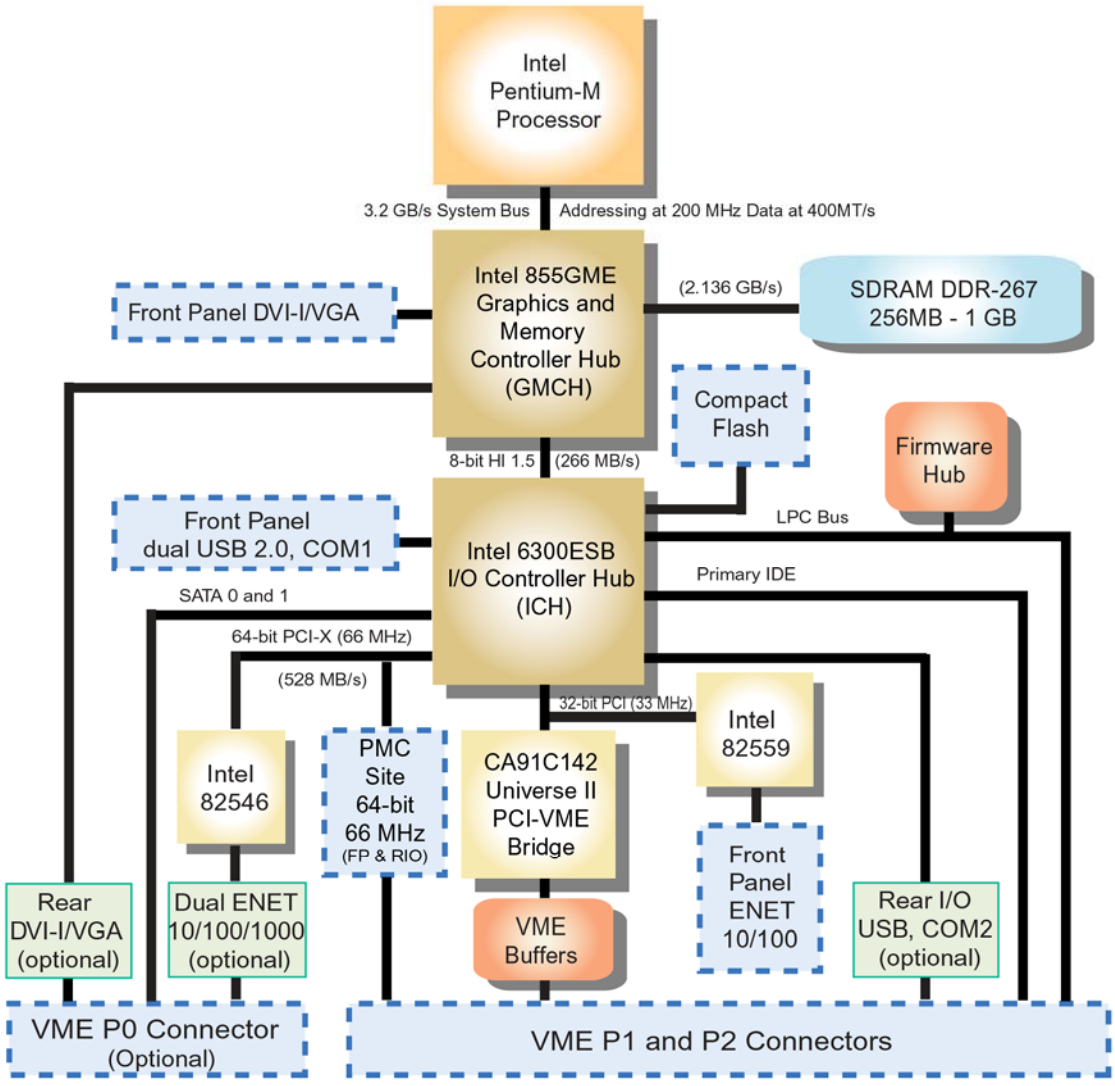
- IEEE Draft Std P1386/2.0, *Draft Standard for a Common Mezzanine Card Family: CMC*
  The Institute of Electrical and Electronic Engineers
  345 East 47th Street
  New York, NY 10017
  (800) 678-4333

- IEEE Draft Std P1386.1/2.0, *Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC*
  The Institute of Electrical and Electronic Engineers
  345 East 47th Street
  New York, NY 10017
  (800) 678-4333

3. Hardware Description

3.1 Overview

The block diagram of the xPM is shown below. The sections that follow describe the major functional blocks of the xPM.



3.2 Processor

The xPM supports a Pentium M processor at 1.4 GHz. The Intel Pentium M processor with 2 MB of L2 cache is meet the current and future demands of high-performance, low-power embedded computing, making it ideal for communications, mobile applications, vehicles, and industrial automation applications. While incorporating advanced processor technology, it remains software-compatible with previous members of the Intel® microprocessor family.

- 400 MHz front side bus.
- 4 MB of L2 cache for fast large-table look-ups: routing tables.
- Advanced branch prediction, Micro-op fusion, Hardware stack manager for faster processing.
- Second-generation Streaming SIMD Extensions (Streaming SIMD Extensions 2) capability adds 144 new instructions, including 128-bit SIMD integer arithmetic and 128-bit SIMD double-precision floating-point operation.
- Fully compatible with existing Intel® Architecture-based software.

For further information on the Pentium M processor available from Intel Corporation, search at:

http://www.intel.com/design/intarch/pentiumm/pentiumm.htm

The Intel® Pentium® M processor was designed from the ground up with a new microarchitecture that delivers high performance with low power consumption. With its 90 nm processing technology and 2 MB of L2 advanced transfer cache, the Pentium M offers more performance per Watt.

The Pentium M also offers a dedicated hardware stack manager that employs sophisticated hardware control for improved stack management, advanced branch prediction capability, and a 400 MHz front side bus to the memory controller hub.

3.3 Chipset

The Intel® 855GME Graphics Memory Controller Hub (GMCH) and Intel® 6300ESB I/O Controller Hub (ICH) chipset create an optimized integrated graphics solution with a 400 MHz system bus and integrated 32-bit 3D core at 133 MHz.

The 855GME (GMCH) provides a 266 MHz interface to DDR RAM (72 bits wide with ECC). The RPM can be populated with one or two banks of DRAM for 512 MB or 1 GB of total memory respectively. The GMCH system memory architecture is optimized to maintain open pages (up to 16-kB page size) across multiple rows. As a result, up to 16 pages across four rows is supported. To complement this, the GMCH will tend to keep pages open within rows, or will only close a single bank on a page miss.

The 855GME also has an advanced integrated graphical display controller. The RPM routes the two available DVO ports; one is accessible from the front panel while the other is brought out through the P0 connector to the system backplane. The DVO ports:

- Provide high-speed, 12-bit interfaces with 165 MHz dot clocks
- Supports DVO devices (TV-Out Encoders, TMDS & LVDS transmitters, etc.) with pixel resolutions up to 1600 x 1200 @ 85 Hz and up to 1048 x 1536 @ 72 Hz
- The two ports can be combined for one 24-bit, 330 MHz interface

- Compliant with DVI Specification 1.0
- Front side system bus bandwidth of 3.2 GB/s (400 MHz).

The 6300ESB I/O Controller Hub (ICH) provides most of the RPM's on-board I/O and it's the RPM's PCI-X expansion bridge. The ICH is designed as a low-power, high-performance I/O hub that features:

- 64-bit @ 66 MHz PCI-X expansion that is used on the RPM for the on-board PMC-X slot, the three Ethernet ports available on the RPM, and for the Universe IID PCI/VMEbus bridge
- Four USB 2.0 compliant ports: two of which are routed to the front panel while the other two may optionally be routed to the P2 connector to the backplane (if the LPC interface (also provided by the IHC) is not routed to the Super I/O device on the RPMPTB rear I/O module)
- Integrated IDE controller supports Ultra 100 DMA Mode Transfers up to 100 MB/sec read cycles and 88.88 MB/sec write cycles for a CompactFlash drive on-board and a primary IDE port that is routed through P2 to the RPMPTB
- Two Serial ATA ports providing 150 MB/sec data rates are routed through P0
- Standard PC functionality like a battery-backed RTC and 256-bytes of CMOS RAM, Power Management Logic, Interrupt Controller, Watchdog Timer, AC'97 CODEC, Integrated 16550 compatible UART's, and multimedia timers based on the 82C54

For further information, see the documents referenced in Section 2

3.4 DRAM

The xPM supports a 72-bit wide, DDR-266 memory interface with memory bandwidth of 2.1 GB/s with ECC. The module can be populated to support 512 MB or 1 GB of DRAM.

3.5 Intel 82546EB Dual Gigabit Ethernet Controller

The xPM supports two 10/100/1000BaseTX channels accessible from the backplane. The Intel 82546EB Dual Port Gigabit Ethernet Controller incorporates two full Gigabit Ethernet MAC and PHY layer functions on a single, compact component. The xPM uses the PCI-X interface of the ICH to control the 82546EB. Therefore, the front side data path to the dual Ethernet port controller is 64 bits at 66 MHz.

The Intel 82546EB offers the following features:

- 10, 100, and 1000BaseTX support with auto-negotiation
- Dual 64KB configurable RX and TX packet FIFOs
- 128-bit internal data path architecture for low latency data handling and superior DMA transfer rate performance
- Built-in Phyceiver
- Serial EEPROM for non-volatile Ethernet address storage

Both 10/100/1000BaseTX ports of the 82546 device are brought out to the P0 backplane connector in compliance with the VITA 31.1 specification. VITA 31.1 lets the user implement fabric switching on the backplane where 31.1 compliant SBC's can communicate with each other and with an external network through switch modules that are

located at either end of the backplane. Optionally these two 1 Gb Ethernet ports are brought to industry standard RJ-45 connectors on Dynatem's rear I/O plug-in module (XPMPTB).

The Intel 82546 contains several PCI configuration registers. It also contains a number of device registers for controlling the Ethernet operation that can be mapped to the memory space or the I/O space. The PCI signals specific to the xPM's 82546 are shown below:

Intel 82546 Signal	PCI Bus Connection
Bus	2
IDSEL	AD18 (Device 2)
PREQ	REQ1#
PGNT	GNT1#
PIRQ for Port A	PX_IRQ2
PIRQ for Port B	PX_IRQ3

3.6 Intel 82559 Fast Ethernet Controller

The Intel 82559 offers the following features:

- 10BaseT and 100BaseTX support with auto-negotiation.
- Independent 3 KB receive and transmit FIFOs.
- Powerful on-chip DMA minimizes CPU overhead with zero wait-state burst transfers to system memory.
- Built-in Phyceiver.
- Serial EEPROM for nonvolatile Ethernet address storage.

The 10BaseT/100BaseTX signals are brought out to J3, an RJ-45 connector on the front panel. The pin-out for J4 is given in Appendix A. Two front panel LEDs are located between the VGA connector and the front panel opening for the PMC module and are controlled by the Ethernet circuitry: D1 is next to the J4 (active) and D2 is closer to the PMC module (link established).

The Intel 82559 contains several PCI configuration registers. It also contains a number of device registers for controlling the Ethernet operation that can be mapped to the memory space or the I/O space. The 82559 is controlled by the PCI interface of the ICH. The PCI signals specific to the Intel 82559 are shown below:

Intel 82559 Signal	PCI Bus Connection
Bus	3
IDSEL	AD16 (PCI Device 0)
PREQ	REQ0#
PGNT	GNT0#
PIRQ	INTF#

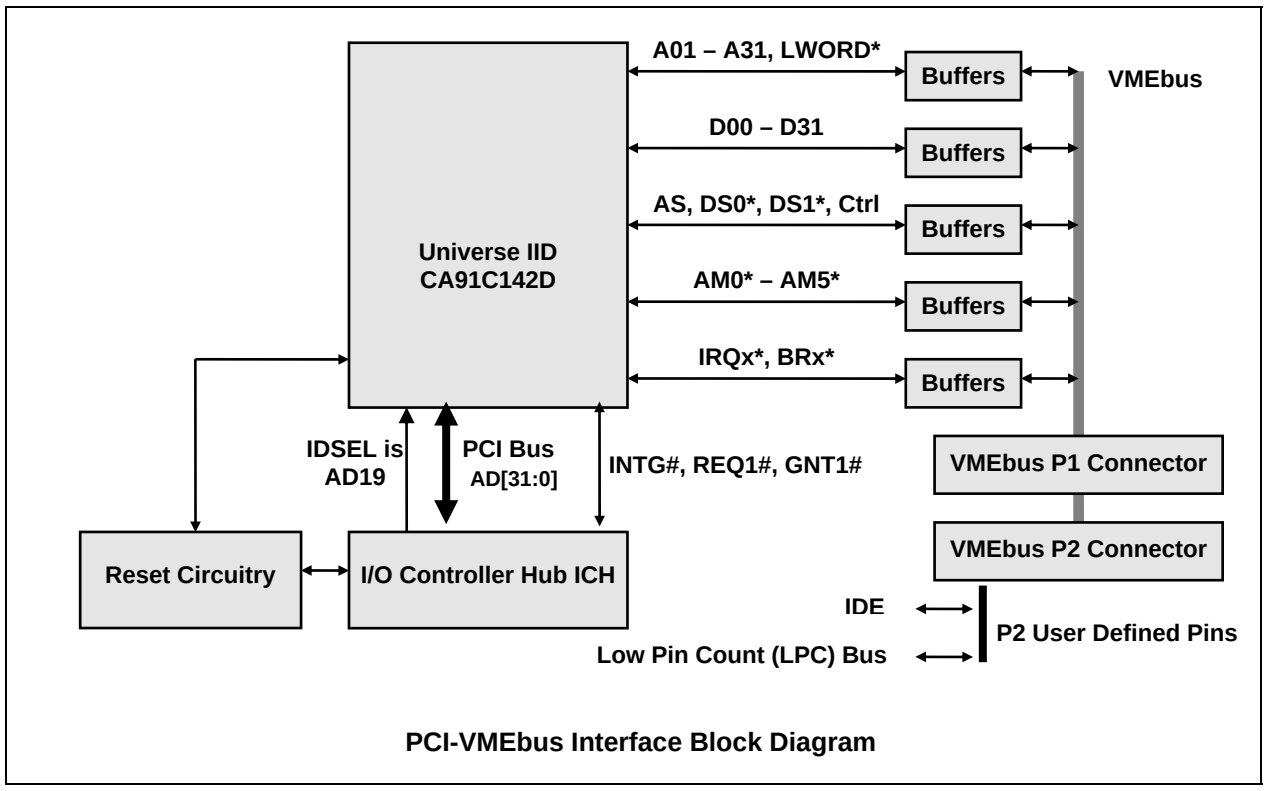
For further information on the 82559, refer to *82559 Fast Ethernet Multifunction PCI/Cardbus Controller*, available from Intel Corporation. Please go to the link at:
http://developer.intel.com/design/network/products/lan/controllers/82559.htm

3.7 Tundra Universe IID CA91C142D PCI-VMEbus Interface

The PCI-VMEbus interface, based on the Tundra Universe IID CA91C142D, offers the following features:

- High-performance 64-bit VMEbus interface.
- Integral FIFOs for write-posting allow the Universe IID to quickly relinquish the bus.
- Programmable DMA controller with linked list support.
- Full VMEbus system controller functionality.
- Complete VMEbus address and data transfer modes: A32/A24/A16 master and slave; D64 (MBLT)/D32/D16/D08 master and slave.

The block diagram of the PCI-VMEbus interface is shown below:



PCI-VMEbus Interface Block Diagram

As shown in the block diagram, several peripheral signals are routed to the user-defined pins of the VMEbus P2 connector: the IDE bus and the LPC bus which routes to a Super I/O chip on the XPMPTB rear plug-in card for I/O expansion. The VMEbus P1 and P2 connector pin-outs are given in Appendix A.

The Universe IID CA91C142D can act as a PCI bus initiator (master) or target (slave), and a VMEbus master or slave. The Universe IID is capable of generating interrupts on the VMEbus, and can act as a VMEbus interrupt handler. The Universe IID provides full VMEbus system controller functionality. The xPM reset circuitry is tied to the Universe IID, since the xPM can generate the VMEbus SYSRESET* signal as well as be reset by another VMEbus board that asserts the SYSRESET* signal. The xPM reset circuitry is discussed in detail in Section 3.12.

This section is intended to supplement the VME-to-PCI Bus Bridge Manual User Manual (downloadable from www.tundra.com), which contains comprehensive descriptions of the operation and programming of the Universe IID. That manual provides the necessary information to understand the operating modes of the Universe IID:

- xPM-initiated transfers (PCI slave, VMEbus master).
- Other VMEbus master-initiated transfers (PCI master, VMEbus slave).
- DMA controller transfers (PCI master, VMEbus master).
- VMEbus interrupt generation.
- VMEbus interrupt handling.
- System controller functionality.
- Register programming via the PCI bus and the VMEbus.
- Coupled and uncoupled transfers between the PCI bus and the VMEbus.
- 4 mailboxes and 8 semaphores.
- VMEbus arbitration.

The Universe IID Control and Status Registers (UCSRs) are used for the configuration of the Universe IID. These registers form a 4 KB block, divided into three groups:

- PCI Configuration Space (PCICS).
- Universe IID Device Specific Status Registers (UDSRs).
- VMEbus Control and Status Registers (VCSRs).

These registers are accessible (to varying degrees) via three address spaces:

- PCI Configuration Space – Only the PCICS register block is accessible in this space.
- PCI Memory Space – The entire 4 KB UCSR block is accessible in this space.
- VMEbus A32/A24/A16 Space – The entire 4 KB UCSR block is accessible in this space.

During initialization, the system BIOS maps PCI peripherals that require space beyond the PCI configuration space into the memory space or I/O space. The Universe IID UCSR block is 4 KB in size and must be aligned on a 64 KB boundary. The total I/O space of an Intel processor is 64 KB and many of the common PC peripherals are found in the first 1 KB of this space. Thus, a request for a 64 KB block of I/O space for the Universe IID registers would be denied by the system BIOS, leaving the Universe IID unmapped. To avoid this situation, the Universe IID offers a power-up option to map its registers into the memory space. This is accomplished on the xPM by tying the VA[1] line high via a pull-up resistor.

There are two mechanisms to access the UCSR block from the VMEbus. The first is the VMEbus Register Access Image (VRAI) method, which is defined by the following registers in the Universe IID *User's Manual*:

Field	Register Bits	Description
Address Space	VAS in Table A.76	A32, A24, or A16
Base Address	BS[31:12] in Table A.77	Lowest address in the 4 KB slave image
Slave Image Enable	EN in Table A.76	Enable VMEbus Register Access Image
Mode	SUPER in Table A.76	Supervisor and/or Non-Privileged
Type	PGM in Table A.76	Program and/or Data

The reset state of the VAS, BS[31:12], and EN fields can be configured as power-up options. On the xPM, all of these fields reset to 0. Thus, the VRAI method must be configured and enabled by accessing the Universe IID registers in the memory space.

The second mechanism for accessing the UCSR block from the VMEbus is the CS/CSR method, which is defined by the following registers in the Universe IID section of the *User's Manual*:

Field	Register Bits	Description
Base Address	BS[23:19] in Table A.84	Base address of Universe IID 512 KB slot
Slave Image Enable	EN in Table A.78	Enable CS/CSR image

The BS[23:19] and EN fields reset to all 0s, and the EN bit can be set by the VME64 Auto ID process. Thus, the CR/CSR method must be configured by accessing the Universe IID registers in the memory space.

The PCI signals specific to the Tundra Universe IID CA91C142D are routed from the PCI bus of the ICH and they are shown below:

Tundra Universe IID CA91C142D Signal	PCI Bus Connection
Bus	3
IDSEL	AD17 (PCI Device 1)
REQ#	REQ1#
GNT#	GNT1#
LINT0#	INTG#
LINT1#	Pulled Up

3.8 PCI-X Mezzanine Card (PMCX) Expansion

The xPM supports one PCI-X Mezzanine Card (PMC-X) site on-board where the I/O can be routed out through the P2 connector (please see Appendix A) or accessed from the front panel. The PMC-X site is compliant with ANSI/VITA 20-2001 for conduction-cooled systems. Conduction cooled PMC-X modules are recommended for use wth the RPM rugged version.

3.9 Intel's FW82802AC Firmware Hub Holds the System BIOS In Flash Memory

The Intel FW82802AC uses a 5-pin interface and provides 1 MByte of flash memory for the system BIOS. This device can fill the 1 MB real mode memory map so only a portion its upper 256 MB is used. The FW82802AC's 1 MB of memory space is segmented into sixteen parameter blocks of 64 KB each. The xPM powers up into real mode and the BIOS is eventually shadowed into system DRAM after booting through the BIOS.

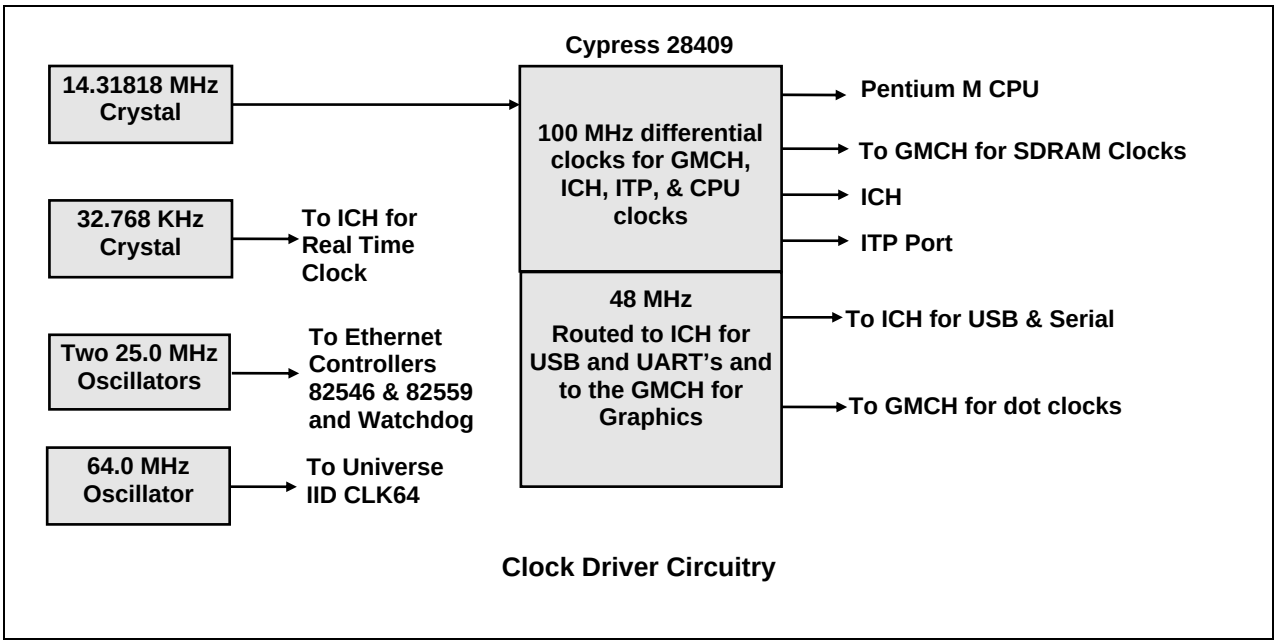
The ICH provides the 5-pin interface to the E82802AC. The upper 256 KB of the E82802AC is located from 000C0000 - 000FFFFF and its full 1 MB of memory is aliased from FFF00000 – FFFFFFFF where it can be fully accessed after booting up through the BIOS.

Here's a link to a datasheet for the 82802AC:

ftp://download.intel.com/design/chipsets/datashts/29065804.pdf

3.10 Clock Drivers

The clock driver circuitry is shown below:

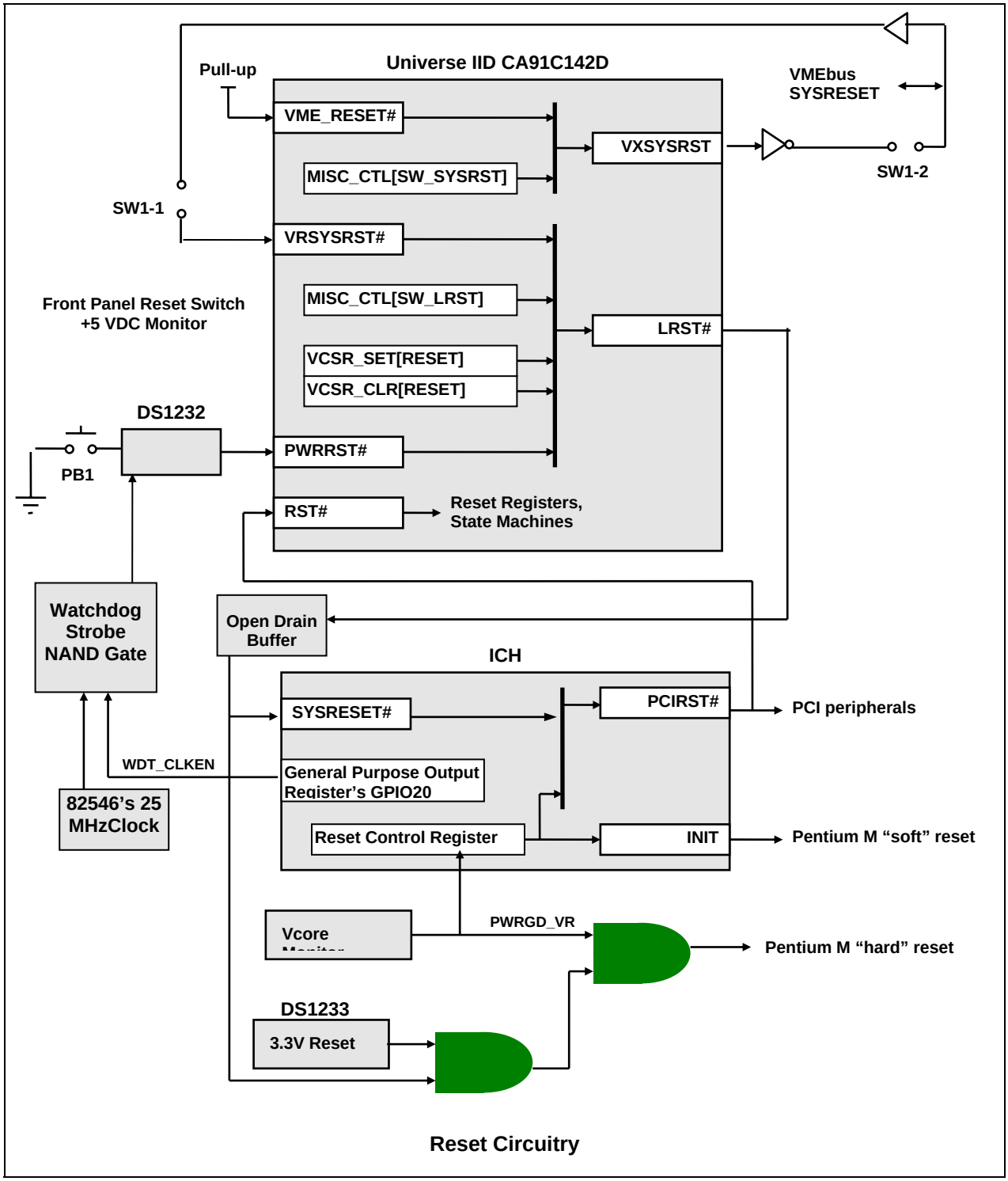


Clock Driver Circuitry

The clocks are generated by the Cypress 28409, which is driven by a 14.31818 MHz crystal. DRAM clocks are synthesized by the GMCH and Hub Interface and PCI(-X) clocks are produced by the ICH. A 32.768 KHz Crystal drives the Real Time Clock (RTC) on the ICH. The Fast Ethernet port provided to the front panel by the 82559 and the two 1 Gb Ethernet ports provided to the backplane by the 82546 require separate 25.0 MHz oscillators (one of the two oscillators is also used for the watchdog timer clock). A 64.0 MHz oscillator drives the Universe IID CA91C142D VMEbus circuitry.

3.11 Reset Circuitry

The reset circuitry is shown below:



Reset Circuitry

There are eight ways to perform a hard reset of the xPM:

- The DS1232 senses that the +5 VDC supply has dropped too low, asserting a PWROK signal to the ICH. This signal resets the processor and the Chipset and, ultimately, all PCI and PCI-X peripherals. The output of the DS1232 runs through the Universe IID (If the board is delivered without the VMEbus interface circuitry (the XHC) this path is replaced with a bypass 0 ohm resistor).

- A DS1233 monitors the on-board 3.3 VDC, regulated from the 5.0 VDC off the backplane, and provides proper power sequencing for the CPU.

- The local on-board voltage regulator for the CPU's core voltage will generate a reset if its output voltage is out of range through signal PWRGD_VR.

- The front panel reset switch, PB1, is pressed, which also asserts a PWROK signal from the DS1232 and resets the xPM.

- Another VMEbus board asserts SYSRESET*, which asserts the Universe IID VRSYSRST# input and, if Jumper SW1-1 is closed, will reset the xPM.

- The SW_SYSRST bit in the MISC_CTL register of the Universe IID is set by code running on the xPM processor. This asserts the VMEbus SYSRESET* signal if SW1-2 is closed. If SW1-1 is open the xPM can reset the VMEbus without resetting itself.

- The SW_LRST bit in the MISC_CTL register of the Universe IID is set by code running on the xPM processor. This performs a local hard reset, via signal LRST#, of the xPM board circuitry. If SW1-2 is open LRST# will reset the xPM without asserting a VMEbus SYSRESET* signal.

- Another VMEbus master sets the RESET bit in the VCSR_SET register of the Universe IID over the VMEbus. In this case the LRST# signals remains asserted until the RESET bit of the VCSR_CLR register of the Universe IID is set by another VMEbus master over the VMEbus.

- The Reset Control Register in the ICH can be set appropriately by code running on the xPM processor.

- Let the watchdog timer time out; see Section 3.12 below.

For further information on the peripherals that play a part in the reset circuitry, refer to ICH datasheet that's referenced in Section 2.

3.12 Watchdog Timer Operation

The xPM's DS1232 if the watchdog timer is enabled and times out.

The xPM's watchdog timer is controlled by one general-purpose output line (GPIO20) that is asserted by the ICH. The DS1232 has a strobe input pin that must see an active clock. If no clock pulse is generated to the pin within 500 milliseconds, the entire xPM board will be reset. As long as GPIO20 is high, a 25 MHz clock will be present at the strobe input.

To use the watchdog timer, drive GPIO20 low, thereby turning off the 25 MHz clock to the DS1232's strobe input, and write a software routine that will bring GPIO20 high before 500 milliseconds elapses. GPIO20 is controlled by bit 20 in the ICH's GP_LVL register. GPIO20 reflects the status of bit 20: GPIO20 is high if bit 20 is at logic 1 and it is low if bit 20 is at logic 0. GPIO20 is high at reset so the watchdog timer will only be activated when the user drives bit 20 of the GP_LVL register low. For instructions on programming the GP_LVL register, refer to the *Intel® 6300ESB I/O Controller Hub Data Sheet* from Intel Corporation, Document # 300641-002.

4. Installation

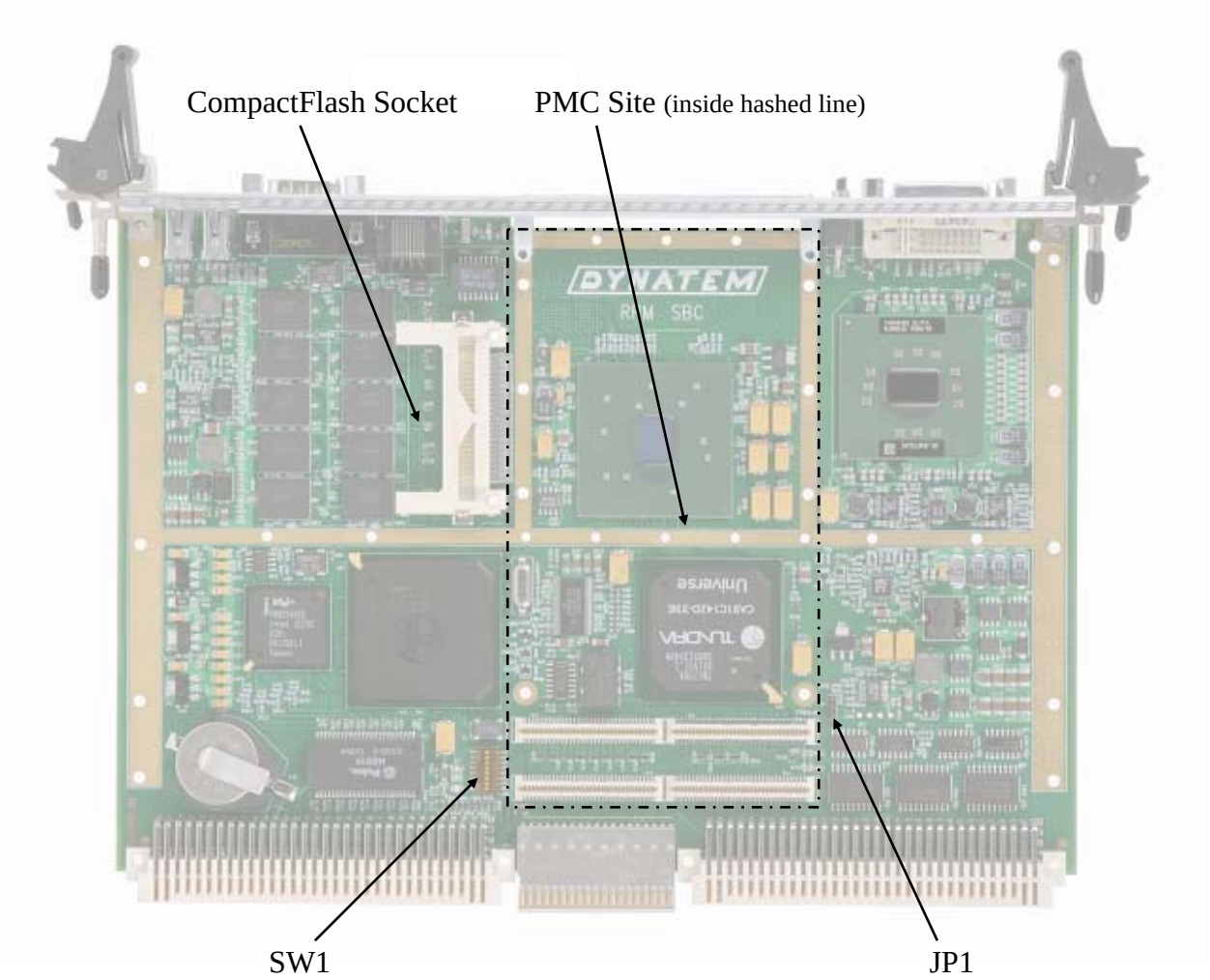
The following sections cover the steps necessary to configure the xPM and install it into a VMEbus system for single-slot operation. This chapter should be read in its entirety before proceeding with the installation.

This section explains how to set up user configurable switches and jumpers and how to install CompactFlash drives and PMC modules.

The xPM is shipped in an antistatic bag. Be sure to observe proper handling procedures during the configuration and installation process, to avoid damage due to electrostatic discharge (ESD).

4.1 Jumper Selectable Options

The xPM contains one jumper and a surface-mount piano switch for system configuration. The jumper, switch, PMC site, and CompactFlash socket are indicated in the photo below:



The xPM offers a number of user configurable hardware options.

Jumpers	Description
JP1	Determines VIO for the PMC site (1 – 2 for 3.3 VDC; 2 – 3 for 5.0 VDC)
SW1-1	xPM is reset by the VMEbus SYSRESET when closed
SW1-2	xPM drives SYSRESET to the VMEbus when closed
SW1-3	VMEbus Slot 1 Controller when open
SW1-4 through SW1-6	Unused
SW1-7	Close momentarily to flush RTC and NV-RAM and revert to BIOS defaults
SW1-8	**MUST STAY CLOSED** (on-board BIOS is disabled when open)
SW2-1 through SW2-4	DDC Routing for DVI-I Interface (set at the factory)

Jumper JP1 selects the VIO routed to the xPM's PMC module. The VIO pins determine the signaling voltage on the PMC module's PCI interface. Refer to the PMC module's reference manual to ascertain the recommended VIO. Shunting pins 1 & 2 of JP1 provides a VIO of 3.3 VDC. Shunting between pins 2 & 3 routes 5 VDC to the VIO pins on the PMC module.

VIO Voltage Level	JP1
3.3 VDC	1-2
5 VDC	2-3

Battery Voltage Supply Selection

Switch SW1-1 lets VMEbus SYSRESET reset the xPM when closed. When open, a VMEbus SYSRESET from other modules will not reset the xPM.

VMEbus SYSRESET In Selection	SW1-1
xPM Won't Receive SYSRESET from the VMEbus	Open
xPM Receives SYSRESET from the VMEbus	Closed

VMEbus SYSRESET In Selection

SW1-2 lets an xPM SYSRESET reset the VMEbus when closed. When open, the xPM cannot drive a SYSRESET to other modules on the VMEbus. The Universe IID only drives SYSRESET when the xPM is a Slot 1 Controller.

VMEbus SYSRESET Out Selection	SW1-2
xPM Won't Drive SYSRESET to the VMEbus	Open
xPM Drives SYSRESET to the VMEbus	Closed

VMEbus SYSRESET Out Selection

When a VMEbus module occupies slot 1 of the VMEbus chassis (the slot to the extreme left), it must operate as system controller (act as multiprocessing arbiter and generate utility bus signals). SW1-3 configures the VMEbus System Controller functionality of the Universe IID, as shown below:

VMEbus System Controller	SW1-3
Enabled	Open
Disabled	Closed

VMEbus System Controller Configuration

Switch SW1-7 is provided for clearing the NVRAM. If BIOS parameters are modified and the xPM goes into a failure mode, default variables can be restored by closing SW1-7for roughly 15 seconds.

4.2 CompactFlash Drive Installation

The xPM supports a bootable CompactFlash Drive for booting up into an Operating System (OS) while occupying only one slot in the VMEbus chassis. Connector J4 is a Type II CompactFlash connector and is used for this purpose. J4 is located behind the front panel Ethernet connector on the xPM's printed circuit board.

4.3 PCI Mezzanine Card (PMC) Installation

The xPM supports one add-on module site that lets the user expand the xPM's local I/O with a PCI Mezzanine Card (PMC) or PMCX (PMC modules capable of PCI-X transfers) module. The PMCX site is backwards compatible and can support any module from 32-bit PMC cards at 33 MHz to 64-bit PMCX modules at 66 MHz.

The PMCX site on the xPM is routed from the ICH's PCI-X bus interface which is 64 bits wide and has a maximum clock rate of 66 MHz The xPM's PCI-X bus interfaces to the 82546 dual Gb Ethernet controller and to the PMCX site.

PMCX site	Available Data Rates with VIO = 5 V (JP1 is shunted between pins 2 & 3)	Available Data Rates with VIO = 3.3 V (JP1 is shunted between pins 1 & 2)
1	33 MHz	33 MHz and 66 MHz

The General Software BIOS will determine during startup what the status is on the installed PMC(X) card. The BIOS monitors the following pins that are routed to the ICH: PCIXCAP (PCX-X capable) and M66EN (66 MHz capable). The user's manual on your PMC(X) modules will tell you how PCIXCAP (JN1, pin 39) and M66EN (JN2, pin 47) are configured.

Conventionally PMC connectors have four designators: JN1 – JN4. JN1 & JN2 provide all the signals necessary for 32-bit PCI transactions, JN3 has the 32 additional data lines required for 64-bit transfers, and JN4 routes I/O off the module for possible backplane access (see Section A for JN4 to P2 backplane PMCX I/O routing). The following table lists the reference designators used on the xPM's PMC(X) site:

PMCX site	JN1	JN2	JN3	JN4
1	P11	P12	P13	P14

4.4 VMEbus Chassis Installation

Unless your VMEbus chassis features automatic daisy chaining, it will have a set of five jumpers for each slot:

- **Interrupt Acknowledge** – IACKIN* and IACKOUT*
- **Bus Grant 0** – BG0IN* and BG0OUT*
- **Bus Grant 1** – BG1IN* and BG1OUT*
- **Bus Grant 2** – BG2IN* and BG2OUT*
- **Bus Grant 3** – BG3IN* and BG3OUT*

These jumpers are typically found between slots, and when configuring a VMEbus chassis, care must be taken to correctly determine the slot affected by the jumpers (the slot to the right of the jumpers). The interrupt acknowledge

is a daisy chain from the board acknowledging the interrupt request to the boards that can issue an interrupt request. The bus grant signals are daisy chains from the system controller, which contains the bus arbiter, to the boards that can request the bus.

Empty VMEbus slots between boards should have all of these jumpers installed. Any slot containing the xPM should have all of these jumpers removed. Any VMEbus slots after the last board in the chassis (that is, the board farthest away from the system controller, which is always in slot 1) do not require these jumpers. For other boards in the VMEbus chassis, refer to their installation instructions for their jumper requirements.

Once the VMEbus chassis jumpers are installed, insert the xPM into its designated slot. With the xPM ejector handles inward, firmly push the xPM into the VMEbus connectors on the chassis. Tighten the screws to the outside of the ejector handles to complete the installation of the xPM in the VMEbus chassis.

4.5 Front Panel Connectors and Reset Switch

The xPM offers front panel connections for DVO/VGA, two USB connectors for two ports, a COM1 port, and an RJ45 connector for a 10/100BaseTX Ethernet port. Install all front panel cables by inserting them into the appropriate connector. COM1 and DVO/VGA cables can be secured to the xPM by tightening their thumbscrews into the connectors' jackscrews. USB and Ethernet mating connectors should snap into place. Mounting hardware for the front panel connectors are isolated from the xPM's digital ground. They are continuous with the front panel itself that, in turn, is common with chassis ground.

The USB ports can be used as Mouse and Keyboard interfaces but the SMM mode should be turned on in the Features menu of the BIOS (see Section 4.6 below) if an Operating System is used that does not have USB drivers (e.g. DOS or VxWorks).

The xPM contains a recessed reset switch, accessible from the front panel. To reset the xPM, press the reset switch using a small screwdriver blade or similar implement.

The Ethernet connector has a pair of indicator LED's built in. These two LED's offer stats on the 10/100BaseTX port provided by the 82559 Ethernet controller on the xPM. Section 3.6 explains the locations of these LED's but they are labeled on the front panel. Here is an explanation of their functionality:

- **Link** – Ethernet link is established when on.
- **Activity** – Ethernet data is being transmitted or received by the xPM when on.

4.6 Entering the BIOS Setup Mode and Udating the BIOS

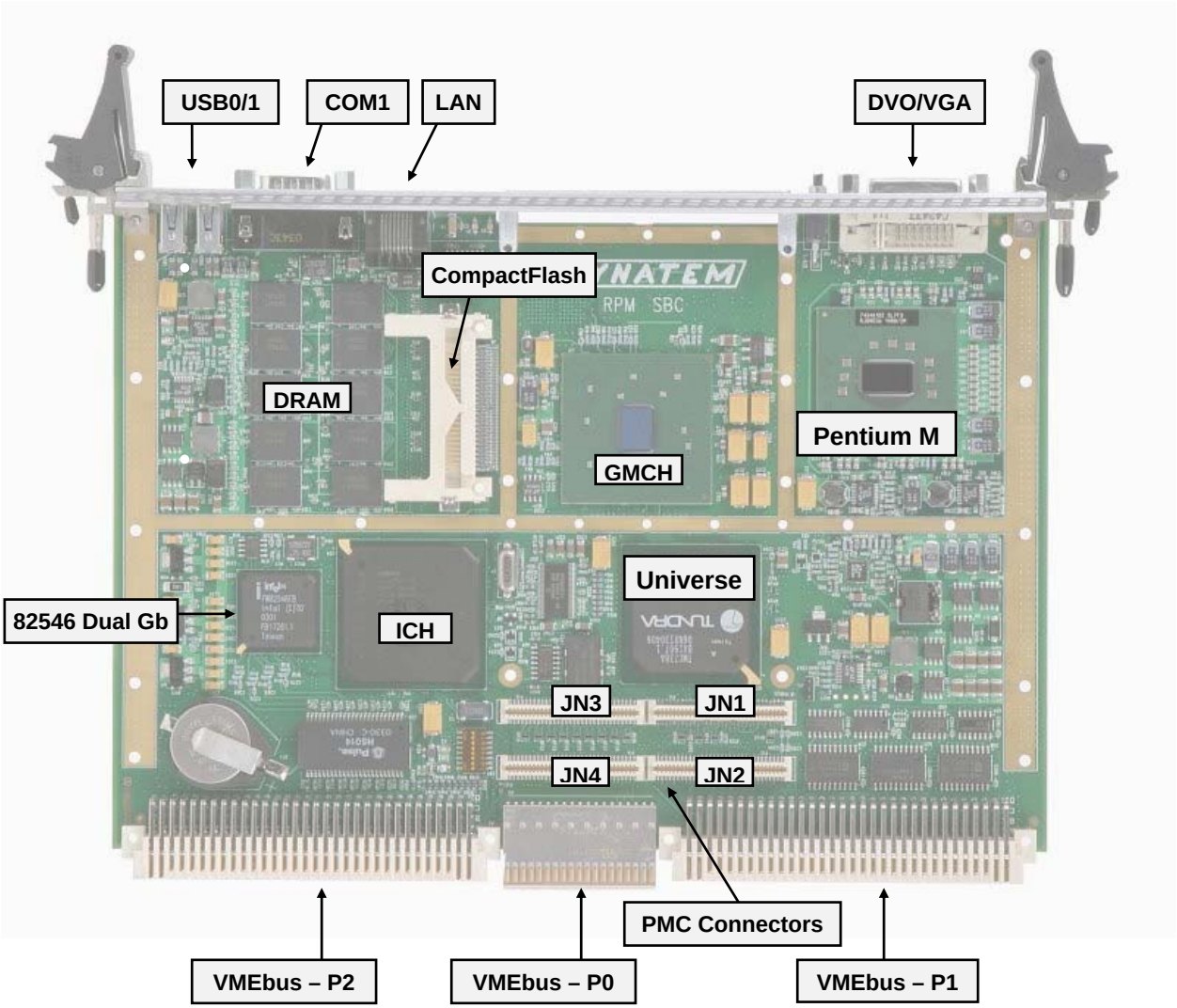
To change the mass storage booting options for the xPM or other BIOS related options, press the <Delete> key on the keyboard after turning power on and the xPM will enter the BIOS Setup Mode. The Setup Mode guides the user with screen prompts.

In the event that the BIOS needs to be modified, this should be done under the guidance of Dynatem's technical staff. Please contact Dynatem at (949)855-3235 or e-mail us at tech@dynatem.com.

The easiest procedure for reprogramming the flash requires the floppy disk interface (connector J3) provided by the XPMPTB described in Appendix B. Contact Dynatem and you will receive a floppy disk image with an executable program that can program your floppy disk with this image. Insert a floppy disk that contains this image in the floppy drive cabled to the XPMPTB. Power up your xPM and enter the BIOS setup mode by pressing <Delete>. In the Features menu, turn off the SMM. Exit the BIOS setup mode and restart the board and the BIOS will be reflashed automatically. When this process has finished, format or discard the floppy disk as it can unintentionally reflash the BIOS in another system.

A. Connector Pin-outs

The locations of the xPM connectors are shown below. The connectors that do not go to the front panel have their pin 1 location designated accordingly.



A.1 DVO/VGA Front Panel Connector (J1)

Both a DVO digital graphics interface and a VGA analog graphics interface are accessible via a DVI-I connector at the front panel. The C signals at the bottom of the table below are the analog VGA signals (with the exception of VSYNC which is on pin 8) while the digital graphics interface is on pins 1 through 24.

Pin	Signal	Pin	Signal	Pin	Signal
1	Data2-	9	Data1-	17	Data0-
2	Data2+	10	Data1+	18	Data0+
3	Signal Ground	11	Signal Ground	19	Signal Ground
4	NC	12	NC	20	NC
5	NC	13	NC	21	NC
6	DDC Clock	14	+5 VDC Power	22	Signal Ground
7	DDC Data	15	Signal Ground	23	Clock+
8	Analog VSYNC	16	HPDET	24	Clock-

Pin	Signal	Pin	Signal
C1	Analog Red	C3	Analog Blue
C5A	Signal Ground	C5	Signal Ground
C2	Analog Green	C4	Analog HSYNC

DVO/VGA Connector (J1) – Front Panel DVI-I Connector. The metal shell of the connector goes to chassis ground.

A.2 COM1 Front Panel Connector (J2)

Connector J2 provides an RS-232 interface at the front panel via a DB-9 connector.

Pin	RS-232 Signals
1	Data Carrier Detect (DCD) Input
2	Received Data (RxD) Input
3	Transmitted Data (TxD) Output
4	Data Terminal Ready (DTR) Output
5	GND
6	Data Set Ready (DSR) Input
7	Request To Send (RTS) Output
8	Clear To Send (CTS) Input
9	Ring Indicator (RI) Input

COM2 Connector (J2) – Front Panel DB9M Connector. The metal shell of the connector goes to chassis ground.

A.3 10/100BaseTX Fast Ethernet Front Panel Connector (J3)

The xPM uses an RJ45 connector to provide an Ethernet port at the front panel.

Pin	Signal Description	Signal Description
1	Port A Transmit Data + (TX+)	TP0+
2	A Transmit Data - (TX-)	TP0-
3	A Receive Data + (RX+)	TP1+
4	Unused	TP2+
5	Unused	TP2-
6	A Receive Data - (RX-)	TP1-
7	Unused	TP3+
8	Unused	TP3-

10BaseT/100BaseTX Fast Ethernet Connector (J3) – Front Panel RJ-45 Connector. The metal shell of the connector goes to chassis ground.

A.4 CompactFlash Interface Connector (J4)

Pin	Signal	Pin	Signal
1	GND	26	CMPFLASHDET
2	D3	27	D11
3	D4	28	D12
4	D5	29	D13
5	D6	30	D14
6	D7	31	D15
7	CS1#	32	CS3#
8	GND	33	No connection
9	GND	34	DIOR#
10	GND	35	DIOW#
11	GND	36	+5 VDC
12	GND	37	DIRQ (IRQ15)
13	+5 VDC	38	+5 VDC
14	GND	39	Pulled Low (master)
15	GND	40	No connection
16	GND	41	IDERESET
17	GND	42	Pulled Up (DIORDY)
18	DA2	43	No connection
19	DA1	44	+5 VDC
20	DA0	45	No connection
21	D0	46	Pull-up to +5 VDC
22	D1	47	D8
23	D2	48	D9
24	No connection	49	D10
25	No connection	50	GND

CompactFlash Type II Interface Connector (J4)

A.5 JTAG Debug Port (J5)

This JTAG connector permits in-circuit emulation for system debugging and is not populated on production boards.

Pin	Signal	Pin	Signal
1	GND	2	GND
3	CPU_BPM0#	4	Pulled Up
5	CPU_BPM1#	6	ITP_RST#
7	CPU_BPM2#	8	GND
9	CPU_BPM3#	10	ITP_TDI
11	CPU_BPM4#/PRDY#	12	ITP_TMS
13	CPU_BPM5#/PREQ#	14	ITP_TRST#
15	FSB_CPURST#	16	ITP_TCK
17	NC	18	Pulled Down
19	ITP_BCLK0	20	GND
21	ITP_BCLK1	22	Pulled Up
23	CPU_BPM5#/PREQ#	24	ITP_TDO
25	GND	26	NC

JTAG Connector (J5)

A.6 Front Panel USB Connector (USB0 & USB1)

There are two USB connectors (labeled P0 and P1) accessible at the XPM's front panel. Though they are separate ports their pin-outs are identical so the following table offers the pin-out of one connector as both.

Pin	Signal Description
1	+5 VDC (via 1.1 amp self-resetting fuse F2)
2	Negative Data
3	Positive Data
4	Signal GND
5	Chassis GND
6	Chassis GND
7	Chassis GND
8	Chassis GND

USB Connectors (USB0 & USB1) – Front Panel USB Receptacles. The metal shell of the connector goes to chassis ground.

A.7 VMEbus Connectors (P1, P2, and P0)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
Z01	NC	A01	D00	B01	BBSY*	C01	D08	D01	+5 VDC
Z02	GND	A02	D01	B02	BCLR*	C02	D09	D02	GND
Z03	NC	A03	D02	B03	ACFAIL*	C03	D10	D03	NC
Z04	GND	A04	D03	B04	BG0IN*	C04	D11	D04	NC
Z05	NC	A05	D04	B05	BG0OUT*	C05	D12	D05	NC
Z06	GND	A06	D05	B06	BG1IN*	C06	D13	D06	NC
Z07	NC	A07	D06	B07	BG1OUT*	C07	D14	D07	NC
Z08	GND	A08	D07	B08	BG2IN*	C08	D15	D08	NC
Z09	NC	A09	GND	B09	BG2OUT*	C09	GND	D09	NC
Z10	GND	A10	SYSCLK	B10	BG3IN*	C10	SYSFAIL*	D10	NC
Z11	NC	A11	GND	B11	BG3OUT*	C11	BERR*	D11	NC
Z12	GND	A12	DS1*	B12	BR0*	C12	SYSRST*	D12	NC
Z13	NC	A13	DS0*	B13	BR1*	C13	LWORD*	D13	NC
Z14	GND	A14	WRITE*	B14	BR2*	C14	AM5	D14	NC
Z15	NC	A15	GND	B15	BR3*	C15	A23	D15	NC
Z16	GND	A16	DTACK*	B16	AM0	C16	A22	D16	NC
Z17	NC	A17	GND	B17	AM1	C17	A21	C17	NC
Z18	GND	A18	AS*	B18	AM2	C18	A20	D18	NC
Z19	NC	A19	GND	B19	AM3	C19	A19	D19	NC
Z20	GND	A20	IACK*	B20	GND	C20	A18	D20	NC
Z21	NC	A21	IACKIN*	B21	No connection (NC)	C21	A17	D21	NC
Z22	GND	A22	IACKOUT*	B22	No connection (NC)	C22	A16	D22	NC
Z23	NC	A23	AM4	B23	GND	C23	A15	D23	NC
Z24	GND	A24	A07	B24	IRQ7*	C24	A14	D24	NC
Z25	NC	A25	A06	B25	IRQ6*	C25	A13	D25	NC
Z26	GND	A26	A05	B26	IRQ5*	C26	A12	D26	NC
Z27	NC	A27	A04	B27	IRQ4*	C27	A11	D27	NC
Z28	GND	A28	A03	B28	IRQ3*	C28	A10	D28	NC
Z29	NC	A29	A02	B29	IRQ2*	C29	A09	D29	NC
Z30	GND	A30	A01	B30	IRQ1*	C30	A08	D30	NC
Z31	NC	A31	-12VDC/NC	B31	+5 VDC Standby	C31	+12VDC/NC	D31	GND
Z32	GND	A32	+5 VDC	B32	+5 VDC	C32	+5 VDC	D32	+5 VDC

VMEbus Connector (P1) – DIN 41612 96-pin (3 rows x 32 pins)

The xPM routes both the primary IDE interface and the Low Pin Count (LPC) bus to the P2 connector's a and c rows while the middle row, row b, is used for the VMEbus' extended address and data bus. The IDE interface is arranged in such a way that a 40-pin flat ribbon cable can be assembled using pin-to-pin routing that would be compatible with an IDE hard drive. A13 on P2 would correspond to pin 1 on an IDE connector while pin C32 would correspond to pin 40. The LPC bus is routed to the backplane so that Dynatem's XPMPTB rear plug-in expansion card can provide standard PC I/O (COM3/4, PS/2 Mouse/Kybd, LPT1, & FDC) with a Super I/O device. The Super I/O device attaches to the xPM via the LPC bus.

Optional versions of the xPM are available that route two USB 2.0 ports and a COM2 RS-232 port to P2 instead of the LPC. This alternative may be useful for customers who do not wish to use the LPC because they have no room for the XPMPTB. These signals are printed in the table below in *italicized red.*

I/O pins from JN4 (connector P14) of the PMCX module are routed to rows d and z.

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
Z01	P14-2	A01	*COM2-DCD*	B01	+5 VDC	C01	+3.3 VDC/*COM2-DSR*	D01	P14-1
Z02	GND	A02	*COM2-RxD*	B02	GND	C02	CLK33_SIO/*COM2-RTS*	D02	P14-3
Z03	P14-5	A03	LAD0/*COM2-TxD*	B03	No Connect	C03	LAD3/*COM2-CTS*	D03	P14-4
Z04	GND	A04	LAD1/*COM2-DTR*	B04	A24	C04	LFRAME#/*COM2-RI*	D04	P14-6
Z05	P14-8	A05	LAD2/*GND*	B05	A25	C05	GND	D05	P14-7
Z06	GND	A06	PCIRST#	B06	A26	C06	SW_ON#	D06	P14-9
Z07	P14-11	A07	INTRUDER#	B07	A27	C07	SPKR	D07	P14-10
Z08	GND	A08	EXT_RST#	B08	A28	C08	GND	D08	P14-12
Z09	P14-14	A09	CLK14_SIO/*USB_V*	B09	A29	C09	SERIRQ/*USB_V*	D09	P14-13
Z10	GND	A10	*USB_2N*	B10	A30	C10	LDRQ0#/*USB_3N*	D10	P14-15
Z11	P14-17	A11	SIO_PME#/*USB_2P*	B11	A31	C11	ICH_A20GATE/*USB_3P*	D11	P14-16
Z12	GND	A12	*GND*	B12	GND	C12	KBRST#/*GND*	D12	P14-18
Z13	P14-20	A13	PRI_RST#	B13	+5 VDC	C13	GND	D13	P14-19
Z14	GND	A14	PDD7	B14	D16	C14	PDD8	D14	P14-21
Z15	P14-23	A15	PDD6	B15	D17	C15	PDD9	D15	P14-22
Z16	GND	A16	PDD5	B16	D18	C16	PDD10	D16	P14-24
Z17	P14-26	A17	PDD4	B17	D19	C17	PDD11	C17	P14-25
Z18	GND	A18	PDD3	B18	D20	C18	PDD12	D18	P14-27
Z19	P14-29	A19	PDD2	B19	D21	C19	PDD13	D19	P14-28
Z20	GND	A20	PDD1	B20	D22	C20	PDD14	D20	P14-30
Z21	P14-32	A21	PDD0	B21	D23	C21	PDD15	D21	P14-31
Z22	GND	A22	NC	B22	GND	C22	NC	D22	P14-33
Z23	P14-35	A23	PDDREQ	B23	D24	C23	GND	D23	P14-34
Z24	GND	A24	PDIOW#	B24	D25	C24	GND	D24	P14-36
Z25	P14-38	A25	PDIOR#	B25	D26	C25	GND	D25	P14-37
Z26	GND	A26	PIORDY	B26	D27	C26	GND	D26	P14-39
Z27	P14-41	A27	PDDACK#	B27	D28	C27	GND	D27	P14-40
Z28	GND	A28	IRQ14	B28	D29	C28	NC	D28	P14-42
Z29	P14-44	A29	PDA1	B29	D30	C29	PRI_DET	D29	P14-43
Z30	GND	A30	PDA0	B30	D31	C30	PDA2	D30	P14-45
Z31	P14-46	A31	PDCS1#	B31	GND	C31	PDCS3#	D31	GND
Z32	GND	A32	NC	B32	+5 VDC	C32	GND	D32	+5 VDC

VMEbus Connector (P2) – 160-pin (5 rows x 32 pins)

Connector P0 routes two Gb Ethernet ports (in compliance with VITA 31.1), the DVI-I interface (when it is not routed to the front panel DVI-I connector J1), and two Serial ATA ports.

The two Gb Ethernet ports occupy rows 2 through 5. The LINK and ACT lines control LED's for the Gb Ethernet ports on the XPMPTB.

DVI signals are preceded with "DVI_", Serial ATA signals are preceded with "SATA", and AC '97 signals are preceded with "AC_".

The P0 connector has been revised twice on the DPM module. Below are three pin-outs that reflect these changes. The first table reflects Rev C modules and the following two tables provide pin-outs for revisions D and E. Your DPM's revision can be determined by checking the Printed Wiring Board (PWB) number etched on the solder side of the module near the bottom of the P2 connector (you will see "P/N: D010 6046 00x" where "x" will be 3, 4 , or 5 depending on whether the revision level is C, D, or E respectively).

Rev C modules routed a Codec interface through P0 and this was later removed. The Codec signals start with an "AC97" prefix. Rev D modules added the LPC interface that's already on P2 and Rev E further added a USB interface.

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A01	NC	B01	NC	C01	NC	D01	NC	E01	NC
A02	LPa_DA+	B02	LPa_DA-	C02	GND	D02	LPa_DC+	E02	LPa_DC-
A03	LPa_DB+	B03	LPa_DB-	C03	GND	D03	LPa_DD+	E03	LPa_DD-
A04	LPb_DA+	B04	LPb_DA-	C04	GND	D04	LPb_DC+	E04	LPb_DC-
A05	LPb_DB+	B05	LPb_DB-	C05	GND	D05	LPb_DD+	E05	LPb_DD-
A06	NC	B06	NC	C06	NC	D06	NC	E06	NC
A07	NC	B07	NC	C07	SATA_LED#	D07	LINKB#	E07	LINKA#
A08	NC	B08	NC	C08	GND	D08	ACT_B#	E08	ACT_A#
A09	NC	B09	NC	C09	SATA1_RXN	D09	GND	E09	GND
A10	NC	B10	NC	C10	SATA1_RXP	D10	AC97_SDOUT	E10	AC97_RST#
A11	NC	B11	NC	C11	GND	D11	GND	E11	GND
A12	NC	B12	NC	C12	SATA1_TXN	D12	AC97_SDIN	E12	AC97_BCLK
A13	NC	B13	NC	C13	SATA1_TXP	D13	GND	E13	GND
A14	NC	B14	NC	C14	GND	D14	NC	E14	AC97_SYNC
A15	DVI_DDCCLK	B15	NC	C15	SATA0_RXP	D15	GND	E15	GND
A16	DVI_DDCDAT	B16	NC	C16	SATA0_RXN	D16	DVI_D2-	E16	DVI_D2+
A17	NC	B17	DVI_BLUE	C17	GND	D17	DVI_CLK-	E17	DVI_CLK+
A18	DVI_VSYNC	B18	DVI_GREEN	C18	SATA0_TXP	D18	DVI_D1+	E18	DVI_D1-
A19	DVI_HSYNC	B19	DVI_RED	C19	SATA0_TXN	D19	DVI_D0-	E19	DVI_D0+

VME64 Extensions Bus Connector (P0) for DPM, Rev C (PWB D010 6046 003) – Row F is grounded

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A01	NC	B01	NC	C01	NC	D01	NC	E01	NC
A02	LPa_DA+	B02	LPa_DA-	C02	GND	D02	LPa_DC+	E02	LPa_DC-
A03	LPa_DB+	B03	LPa_DB-	C03	GND	D03	LPa_DD+	E03	LPa_DD-
A04	LPb_DA+	B04	LPb_DA-	C04	GND	D04	LPb_DC+	E04	LPb_DC-
A05	LPb_DB+	B05	LPb_DB-	C05	GND	D05	LPb_DD+	E05	LPb_DD-
A06	NC	B06	NC	C06	NC	D06	NC	E06	NC
A07	NC	B07	NC	C07	NC	D07	LINKB#	E07	LINKA#
A08	GND	B08	GND	C08	GND	D08	ACT_B#	E08	ACT_A#
A09	GND	B09	DVI_D0-	C09	DVI_D0+	D09	DVI_CLK-	E09	DVI_CLK+
A10	GND	B10	DVI_D1+	C10	DVI_D1-	D10	DVI_D2-	E10	DVI_D2+
A11	NC	B11	GND	C11	GND	D11	GND	E11	GND
A12	NC	B12	GND	C12	NC	D12	GND	E12	SATA0_TXN
A13	NC	B13	GND	C13	SATA_LED#	D13	PCI_RST1#	E13	SATA0_TXP
A14	NC	B14	GND	C14	A20GATE	D14	LAD3	E14	SATA0_RXN
A15	DVI_DDCCLK	B15	NC	C15	CLK14_SIO	D15	LAD2	E15	SATA0_RXP
A16	DVI_DDCDAT	B16	NC	C16	LDRQ0#	D16	LAD1	E16	SATA1_TXP
A17	NC	B17	DVI_BLUE	C17	SIO_PME#	D17	LAD0	E17	SATA1_TXN
A18	DVI_VSYNC	B18	DVI_GREEN	C18	SER_IRQ	D18	LFRAME#	E18	SATA1_RXP
A19	DVI_HSYNC	B19	DVI_RED	C19	KBRST#	D19	CLK33_SIO	E19	SATA1_RXN

VME64 Extensions Bus Connector (P0) for DPM, Rev D (PWB D010 6046 004) – Row F is grounded

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A01	NC	B01	NC	C01	NC	D01	NC	E01	NC
A02	LPa_DA+	B02	LPa_DA-	C02	GND	D02	LPa_DC+	E02	LPa_DC-
A03	LPa_DB+	B03	LPa_DB-	C03	GND	D03	LPa_DD+	E03	LPa_DD-
A04	LPb_DA+	B04	LPb_DA-	C04	GND	D04	LPb_DC+	E04	LPb_DC-
A05	LPb_DB+	B05	LPb_DB-	C05	GND	D05	LPb_DD+	E05	LPb_DD-
A06	NC	B06	NC	C06	NC	D06	NC	E06	NC
A07	NC	B07	NC	C07	NC	D07	LINKB#	E07	LINKA#
A08	GND	B08	GND	C08	GND	D08	ACT_B#	E08	ACT_A#
A09	GND	B09	DVI_D0-	C09	DVI_D0+	D09	DVI_CLK-	E09	DVI_CLK+
A10	GND	B10	DVI_D1+	C10	DVI_D1-	D10	DVI_D2-	E10	DVI_D2+
A11	NC	B11	GND	C11	GND	D11	GND	E11	GND
A12	USB3N	B12	GND	C12	NC	D12	GND	E12	SATA0_TXN
A13	USB3P	B13	GND	C13	SATA_LED#	D13	PCI_RST1#	E13	SATA0_TXP
A14	NC	B14	GND	C14	A20GATE	D14	LAD3	E14	SATA0_RXN
A15	DVI_DDCCLK	B15	NC	C15	CLK14_SIO	D15	LAD2	E15	SATA0_RXP
A16	DVI_DDCDAT	B16	NC	C16	LDRQ0#	D16	LAD1	E16	SATA1_TXP
A17	NC	B17	DVI_BLUE	C17	SIO_PME#	D17	LAD0	E17	SATA1_TXN
A18	DVI_VSYNC	B18	DVI_GREEN	C18	SER_IRQ	D18	LFRAME#	E18	SATA1_RXP
A19	DVI_HSYNC	B19	DVI_RED	C19	KBRST#	D19	CLK33_SIO	E19	SATA1_RXN

VME64 Extensions Bus Connector (P0) for DPM, Rev E (PWB D010 6046 005) – Row F is grounded

A.8 PCI-X Mezzanine Card (PMCX) Connectors (JN1, JN2, JN3, and JN4)

This section has the pin-outs for all four PMC connectors.

Pin	Signal	Pin	Signal
1	5.6K pull-down	2	-12 VDC
3	GND	4	PX_PIRQ0#
5	PX_PIRQ1#	6	PX_PIRQ2#
7	No connection	8	+5 VDC
9	PX_PIRQ3#	10	No connection
11	GND	12	No connection
13	PCI CLK	14	GND
15	GND	16	GNT0#
17	REQ0#	18	+5 VDC
19	VI/O	20	AD31
21	AD28	22	AD27
23	AD25	24	GND
25	GND	26	C/BE3#
27	AD22	28	AD21
29	AD19	30	+5 VDC
31	VI/O	32	AD17
33	FRAME#	34	GND
35	GND	36	IRDY#
37	DEVSEL#	38	+5 VDC
39	PCIXCAP	40	LOCK#
41	No connection	42	No connection
43	PAR	44	GND
45	VI/O	46	AD15
47	AD12	48	AD11
49	AD9	50	+5 VDC
51	GND	52	C/BE0#
53	AD6	54	AD5
55	AD4	56	GND
57	VI/O	58	AD3
59	AD2	60	AD1
61	AD0	62	+5 VDC
63	GND	64	REQ64#

PCI-X Mezzanine Card (PMCX) Connector (JN1) – Molex 71439-0164

VIO is jumper selectable (through JP1, please see Section 4.1).

Pin	Signal	Pin	Signal
1	+12 VDC	2	TRST (pulled down)
3	TMS (pulled up)	4	No connection
5	TDI (pulled up)	6	GND
7	GND	8	No connection
9	No connection	10	No connection
11	+3.3 VDC	12	+3.3 VDC
13	PCI RST#	14	GND
15	+3.3 VDC	16	GND
17	No connection	18	GND
19	AD30	20	AD29
21	GND	22	AD26
23	AD24	24	+3.3 VDC
25	AD17 (IDSEL)	26	AD23
27	+3.3 VDC	28	AD20
29	AD18	30	GND
31	AD16	32	C/BE2#
33	GND	34	No connection
35	TRDY#	36	+3.3 VDC
37	GND	38	STOP#
39	PERR#	40	GND
41	+3.3 VDC	42	SERR#
43	C/BE1#	44	GND
45	AD14	46	AD13
47	M66EN	48	AD10
49	AD8	50	+3.3 VDC
51	AD7	52	No connection
53	+3.3 VDC	54	No connection
55	No connection	56	GND
57	No connection	58	No connection
59	GND	60	No connection
61	ACK64#	62	+3.3 VDC
63	GND	64	No connection

PCI-X Mezzanine Card (PMCX) Connector (JN2) – Molex 71439-0164

Pin	Signal	Pin	Signal
1	No connection	2	GND
3	GND	4	C/BE7#
5	C/BE6#	6	C/BE5#
7	C/BE4#	8	GND
9	VIO	10	PAR64
11	AD63	12	AD62
13	AD61	14	GND
15	GND	16	AD60
17	AD59	18	AD58
19	AD57	20	GND
21	VIO	22	AD56
23	AD55	24	AD54
25	AD53	26	GND
27	GND	28	AD52
29	AD51	30	AD50
31	AD49	32	GND
33	GND	34	AD48
35	AD47	36	AD46
37	AD45	38	GND
39	VIO	40	AD44
41	AD43	42	AD42
43	AD41	44	GND
45	GND	46	AD40
47	AD39	48	AD38
49	AD37	50	GND
51	GND	52	AD36
53	AD35	54	AD34
55	AD33	56	GND
57	VIO	58	AD32
59	No connection	60	No connection
61	No connection	62	GND
63	GND	64	No connection

PCI-X Mezzanine Card (PMCX) Connector (JN3) – Molex 71439-0164

Pin	Signal	Pin	Signal
1	D1	2	Z1
3	D2	4	D3
5	Z3	6	D4
7	D5	8	Z5
9	D6	10	D7
11	Z7	12	D8
13	D9	14	Z9
15	D10	16	D11
17	Z11	18	D12
19	D13	20	Z13
21	D14	22	D15
23	Z15	24	D16
25	D17	26	Z17
27	D18	28	D19
29	Z19	30	D20
31	D21	32	Z21
33	D22	34	D23
35	Z23	36	D24
37	D25	38	Z25
39	D26	40	D27
41	Z27	42	D28
43	D29	44	Z29
45	D30	46	Z31
47	No connection	48	No connection
49	No connection	50	No connection
51	No connection	52	No connection
53	No connection	54	No connection
55	No connection	56	No connection
57	No connection	58	No connection
59	No connection	60	No connection
61	No connection	62	No connection
63	No connection	64	No connection

PCI-X Mezzanine Card (PMCX) Site #1 Connector (JN4) – Molex 71439-0164

JN4 is labeled P14. These I/O lines are optionally routed to the VMEbus backplane on the listed P2 pins.

B. Address Maps, Interrupts, DMA Channels

Tables of the xPM's address maps, interrupt request assignments, and DMA channel usage are given in the following sections. All addresses are shown in hexadecimal notation.

B.1 Memory Map

The xPM's memory map is shown below:

Address Range	Description
00000000 – 000FFFFF	DOS legacy address range
00100000 - Top of On-board DDR SDRAM Memory	On-board DDR DRAM 1GB
Top of On-board DRAM Memory – FEBFFFFF	PCI Device Allocation
FEC00000 - FEEFFFFF	APIC Configuration Area (unused on xPM)
FFE00000 - FFFFFFFF	High BIOS Area

This is the memory map on the GMCH.

For further details on the xPM memory space map, refer to Section 5.1 in *Intel's 855GM/855GME Chipset Graphics and Memory Controller Hub(GMCH) Datasheet*, Document # 252615-004, available from Intel Corporation.

B.2 PCI Configuration Space Map

The PCI configuration space map will vary if the PMCX expansion slot is used to support a PMCX add-on mezzanine card and if that PMCX module uses a expansion bridge designed for multiple targets on the secondary bus. This is an extremely unlikely situation but the bus numbers in this condition will differ from those provided in the following table. The Vendor ID and Device ID in hex for the PMCX slot are shown as *xxxx*, since they depend on the type of device installed in the PMC slot.

IDSEL	Bus	Dev	Fcn	VenID	DevID	Description
—	00	30	0	8086	244E	6300ESB (ICH) P2P Bridge
—	00	31	0	8086	25A1	6300ESB (ICH) P2L Bridge
—	00	31	1	8086	25A2	6300ESB (ICH) PCI-IDE Interface
—	00	31	2	8086	25A3	6300ESB (ICH) SATA Interface
—	00	31	3	8086	25A4	6300ESB (ICH) SMBus Interface
—	00	29	0	8086	25A9	6300ESB (ICH) PCI-USB#0 Interface
—	00	29	1	8086	25AA	6300ESB (ICH) PCI-USB#1 Interface
—	00	29	5	8086	25AC	6300ESB (ICH) APIC
AD16	03	0	0	8086	1229	82559 Fast Ethernet Controller
AD17	03	1	0	10E3	0000	Universe IID CA91C142D PCI-VMEbus Interface
AD18	02	2	0	8086	1010	82546 Gb Ethernet Controller
—	00	2	0	8086	3582	GMCH-integrated Graphics Controller
AD17	02	1	0	xxxx	xxxx	PMCX Site for an Add-on Mezzanine Card

PCI Configuration

B.3 Interrupt Request Routing

The interrupt request routing is shown below:

IRQ	Description
0	Timer 0 (ICH)
1	Keyboard (SMSC's LPC47B272*)
2	Cascade Interrupt from slave PIC (ICH)
3	COM2/COM4 (LPC47B272)
4	COM1/COM3 (LPC47B272)
5	LPT2 (LPC47B272)
6	Floppy Drive (LPC47B272)
7	LPT1 (LPC47B272)
8	Real Time Clock (ICH)
9	No connection (pulled up via 8.2K)
10	No connection (pulled up via 8.2K)
11	No connection (pulled up via 8.2K)
12	Mouse (LPC47B272's kybd/mouse controller)
13	Math Coprocessor (ICH)
14	Primary IDE Interface via P2 connector (ICH)
15	Secondary IDE Interface (CompactFlash) (ICH)

*The LPC47B272 is found on the optional xPMPTB rear I/O expansion card, it is not included with the xPM.

The PCI interrupt request routing to the Intel 6300ESB I/O Controller Hub (ICH) is shown below:

PCI IRQ	Description
PIRQA#	USB 0
PIRQB#	82546EB
PIRQC#	GMCH-integrated SVGA Controller
PIRQD#	USB 1, Universe IID CA91C142D LINT0#

.

For further details on interrupts, refer to the documentation for the various peripherals that generate interrupts, as well as *Intel 6300ESB I/O Controller Hub Datasheet*, Document #300641-002.

C. Power and Environmental Requirements

The xPM power and environmental requirements are shown in the tables below.

Condition	Power Requirements
1.4 GHz Pentium M	+5 VDC @ 3.0 A typ. 3.0 VDC Lithium Coin Cell @ 3.4 µA

Power Requirements

The 3 Volt lithium coin cell is a CR2032 with 190 mAhours capacity and it is used to battery-back the Real Time Clock, the 2 MB of NV-SRAM, and the BIOS's NV-RAM. At 3.4 µA this battery should last for over six years with power off.

Condition	Environmental Requirements
Operating Temperature	-40° to 85° with screening
Storage Temperature	-50° to +105° C

Environmental Requirements

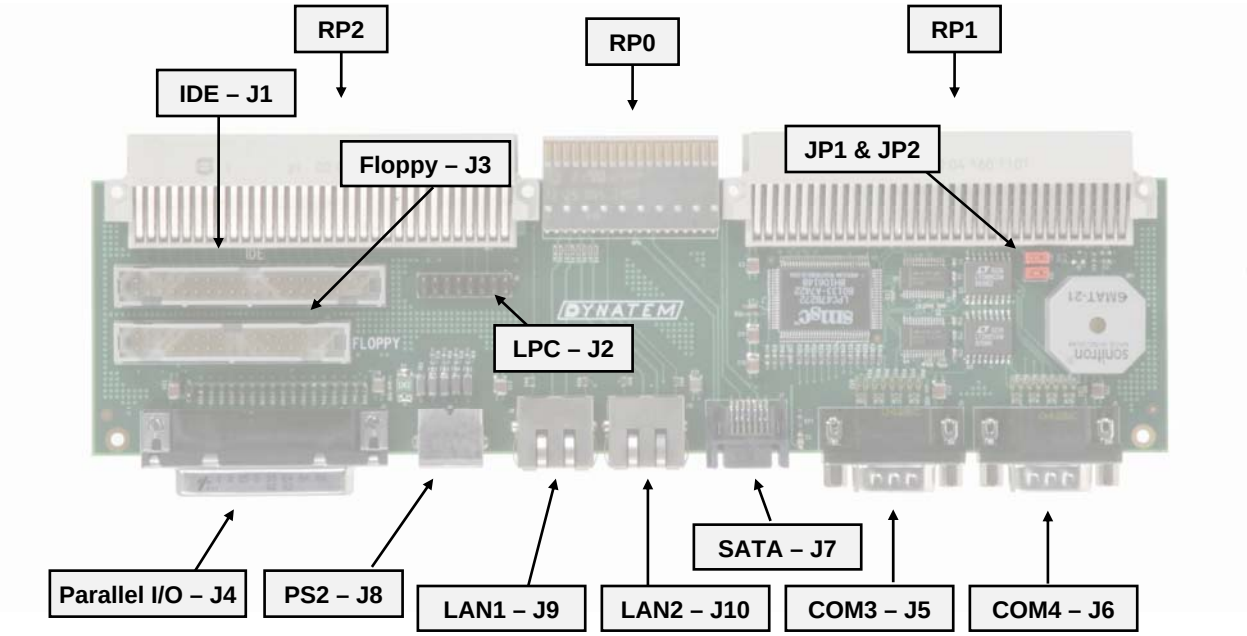
D. XPMPTB Rear Plug-in I/O Expansion Module for the xPM

Dynatem offers a rear plug-in paddle card for I/O expansion with the xPM. Essentially the XPMPTB routes the xPM's Primary IDE interface to an industry standard 40-pin connector and it routes the Low Pin Count (LPC) bus to a Super I/O device that provides COM3/4, LPT1, Floppy Disk Controller (FDC), and P/S2 Mouse/Keyboard interfaces, also made available through industry standard connectors. The IDE and LPC busses are routed to the XPMPTB through the VMEbus backplane's P2 connector.

Two Serial ATA ports are routed through RP0. The XPMPTB also routes two VITA 31.1 compliant 1 Gb Ethernet ports from RP0 to two industry standard connectors for situations where VITA 31.1 backplane fabric switching is not used.

The Super I/O device used for COM3/4, P/S2 Mouse/Keyboard, LPT1, and FDC is SMSC's LPC47B272 and a data sheet can be found at: http://www.smsc.com/main/catalog/lpc47b27x.html

Here is a photograph of the XPMPTB with the connectors indicated:



D.1 XPMPTB Connector Pinouts

Pin	Signal	Pin	Signal
1	RST#	2	GND
3	D7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	GND	20	No connection
21	DMARQ0	22	GND
23	IOW#	24	GND
25	IOR#	26	GND
27	IORDY	28	470-ohm pull-down
29	DMAACK0	30	GND
31	IRQ14	32	No connection
33	DA1	34	No connection
35	DA0	36	DA2
37	CS1Fx	38	CS3Fx
39	LED Control	40	GND

Primary IDE Interface Connector (J1) – 40-pin Dual-row 0.1” Header

Pin	Signal	Pin	Signal
1	SCLK1	2	GND
3	SDAT1	4	CLK33_SIO
5	LAD0	6	LAD3
7	LAD1	8	LFRAME#
9	LAD2	10	GND
11	PCIRST#	12	NC
13	NC	14	NC
15	ITP_RST#	16	GND

Low Pin Count (LPC) Bus Interface Connector (J2)

Pin	Signal	Pin	Signal
1	GND	2	DRVEN0
3	GND	4	No connection
5	No connection	6	DRVEN1
7	GND	8	INDEX#
9	GND	10	MTR0#
11	GND	12	No connection
13	GND	14	DS0#
15	GND	16	No connection
17	GND	18	DIR#
19	GND	20	STEP#
21	GND	22	WDATA#
23	GND	24	WGATE#
25	GND	26	TRK0#
27	GND	28	WRTPRT#
29	GND	30	RDATA#
31	GND	32	HDSEL#
33	GND	34	DSKCHG#

Floppy Disk Controller Interface Connector (J3) – 34-pin Dual-row 0.1” Header

Pin	Signal
1	LPT_STROBE#
2	LPT_PDR0
3	LPT_PDR1
4	LPT_PDR2
5	LPT_PDR3
6	LPT_PDR4
7	LPT_PDR5
8	LPT_PDR6
9	LPT_PDR7
10	LPT_ACK#
11	LPT_BUSY#
12	LPT_PE
13	LPT_SLCT
14	LPT_ALFR#
15	LPT_ERR#
16	LPT_INITR#
17	LPT_INITR#
18	GND
19	GND
20	GND
21	GND
22	GND
23	GND
24	GND
25	GND

LPT1 Parallel Printer Interface Connector (J4) –DB25F Connector

COM3 and COM4 ports can be configured for either RS-232 or RS-422 (or RS-485) operation. Jumpers JP2 and JP1 select the communication mode of ports COM3 and COM4 respectively. Shunting jumper JP2 will put COM3 in RS-232 mode while leaving it unshunted will select RS-4xx operation. JP1 does the same for the COM4 port.

Pin	RS-232 Signals (JP2 Shunted)	RS-4xx Signals
1	Data Carrier Detect (DCD) Input	-TxD
2	Received Data (RxD) Input	-RTS
3	Transmitted Data (TxD) Output	+CTS
4	Data Terminal Ready (DTR) Output	+RxD
5	GND	GND
6	Data Set Ready (DSR) Input	+TxD
7	Request To Send (RTS) Output	+RTS
8	Clear To Send (CTS) Input	-CTS
9	Ring Indicator (RI) Input	-RxD

COM3 Connector (J5) – DB9M Connector. The metal shell of the connector goes to chassis ground.

Pin	RS-232 Signals (JP1 Shunted)	RS-4xx Signals
1	Data Carrier Detect (DCD) Input	-TxD
2	Received Data (RxD) Input	-RTS
3	Transmitted Data (TxD) Output	+CTS
4	Data Terminal Ready (DTR) Output	+RxD
5	GND	GND
6	Data Set Ready (DSR) Input	+TxD
7	Request To Send (RTS) Output	+RTS
8	Clear To Send (CTS) Input	-CTS
9	Ring Indicator (RI) Input	-RxD

COM4 Connector (J6) – DB9M Connector. The metal shell of the connector goes to chassis ground.

J7 is a dual-port stacked Serial ATA connector where both ports have the following pinout:

Pin	Signal
1	GND
2	A+
3	A-
4	GND
5	B-
6	B+
7	GND

Serial ATA Connector (J7) - Pin-out for one port of the dual-stacked connector, Molex Part# 67811-0515

Pin	Signal Description
1	Keyboard Data
2	Mouse Data
3	GND
4	+5 VDC (via 1 amp self-resetting fuse F1)
5	Keyboard Clock
6	Mouse Clock

Keyboard/Mouse Connector (J8) – Mini-DIN Receptacle. The metal shell of the connector goes to chassis ground.

The xPMPTB uses a dual RJ45 connector package to provide two 1 Gb Ethernet ports. These ports are otherwise routed to the P0 connector in compliance with VITA 31.1.

J9		
Pin	**10/100 Signal Description**	**Gb Signal Description**
A1	Port A Transmit Data + (TX+)	TP0+
A2	A Transmit Data - (TX-)	TP0-
A3	A Receive Data + (RX+)	TP1+
A4	Unused	TP2+
A5	Unused	TP2-
A6	A Receive Data - (RX-)	TP1-
A7	Unused	TP3+
A8	Unused	TP3-
J10		
Pin	**10/100 Signal Description**	**Gb Signal Description**
B1	Port B Transmit Data + (TX+)	TP0+
B2	B Transmit Data - (TX-)	TP0-
B3	B Receive Data + (RX+)	TP1+
B4	Unused	TP2+
B5	Unused	TP2-
B6	B Receive Data - (RX-)	TP1-
B7	Unused	TP3+
B8	Unused	TP3-

10BaseT/100BaseTX Fast Ethernet Connector (J9/J10) – Dual RJ-45 Connector. The metal shell of the connector goes to chassis ground.